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SPACE VEHICLE ONBOARD COMMAND ENCODER
FINAL REPORT

ER75-4458

17 DECEMBER 1975

PREPARED UNDER

NASA CONTRACT NO. NAS 9-14372

RAYTHEON

RAYTHEON COMPANY
EQUIPMENT DIVISION



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HOUSTON, TEXAS

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EQUIPMENT DEVELOPMENT LABORATORY

SUDBURY, MASSACHUSETTS 01776



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I. INTRODUCTION

This report defines the design and implementation of a space vehicle onboard Command Encoder brassboard, and test set.

Background

The requirement to generate commands onboard a manned space vehicle for transmission to another space vehicle has not been implemented in any of the manned space programs to date. The advent of vehicles like the Shuttle and space station with the capability to deploy, retrieve, and control a variety of detached payloads and satellites necessitates the development of an onboard command encoder.

The primary function of the Command Encoder is to accept input commands, generated either locally onboard the Space Shuttle or remotely from the ground, format and encode the commands in accordance with the payload's input requirements and appropriately modulate a subcarrier for transmission by the baseband rf modulator. Figure 1-1 depicts a simplified block diagram of the Command Encoder's interfaces. Onboard commands are generated onboard the Shuttle and routed by the Auxiliary Computer to the Command Encoder; while ground originated commands are received via the Uplink channel and moved through the Auxiliary Computer to the Command Encoder. (Note: It is assumed that the data bus feeding the Command Encoder is under control of the Auxiliary Computer.) The Command Encoder accepts the commands on a priority basis and outputs them to the appropriate payload via the crosslink channel. The payload, in turn, acknowledges the command by transmitting either an acknowledgement or bit-by-bit validation message, via the telemetry link and Performance Monitor System (PMS), back to the Command Encoder where the status of each message block is kept. Also available is an internal bit-by-bit validation path (echo check) to enhance message transmission error detection.

To be effective, the onboard encoder must be compatible with the command systems and techniques currently used/or to be used by NASA and other government organizations. These systems are currently implemented in ground hardware operating in controlled environments. Under NASA contract NAS 9-18498, Space Shuttle Onboard Command Encoder Design Definition Study, a flexible encoder system was designed. This report covers the implementation of the encoder design into hardware to demonstrate the various encoding algorithms/code formats, and modulation techniques in a single hardware package, to maintain comparable reliability and link integrity of the existing command systems, and to integrate the various techniques into a single design using current technology.

References

Final Report - Space Shuttle Onboard Command Encoder Design Definition Study (ER73-4525), 12/15/73

Proposal For - Space Vehicle Onboard Command Encoder Volume 1, 10/24/74

Sales Order - Section A, SO Number 81364, Contract NAS 9-14372, 1/20/75.

Section II, Part A of this document, covers the Command Encoder system design, while Part B defines the brassboard hardware design. Parts C and D cover the

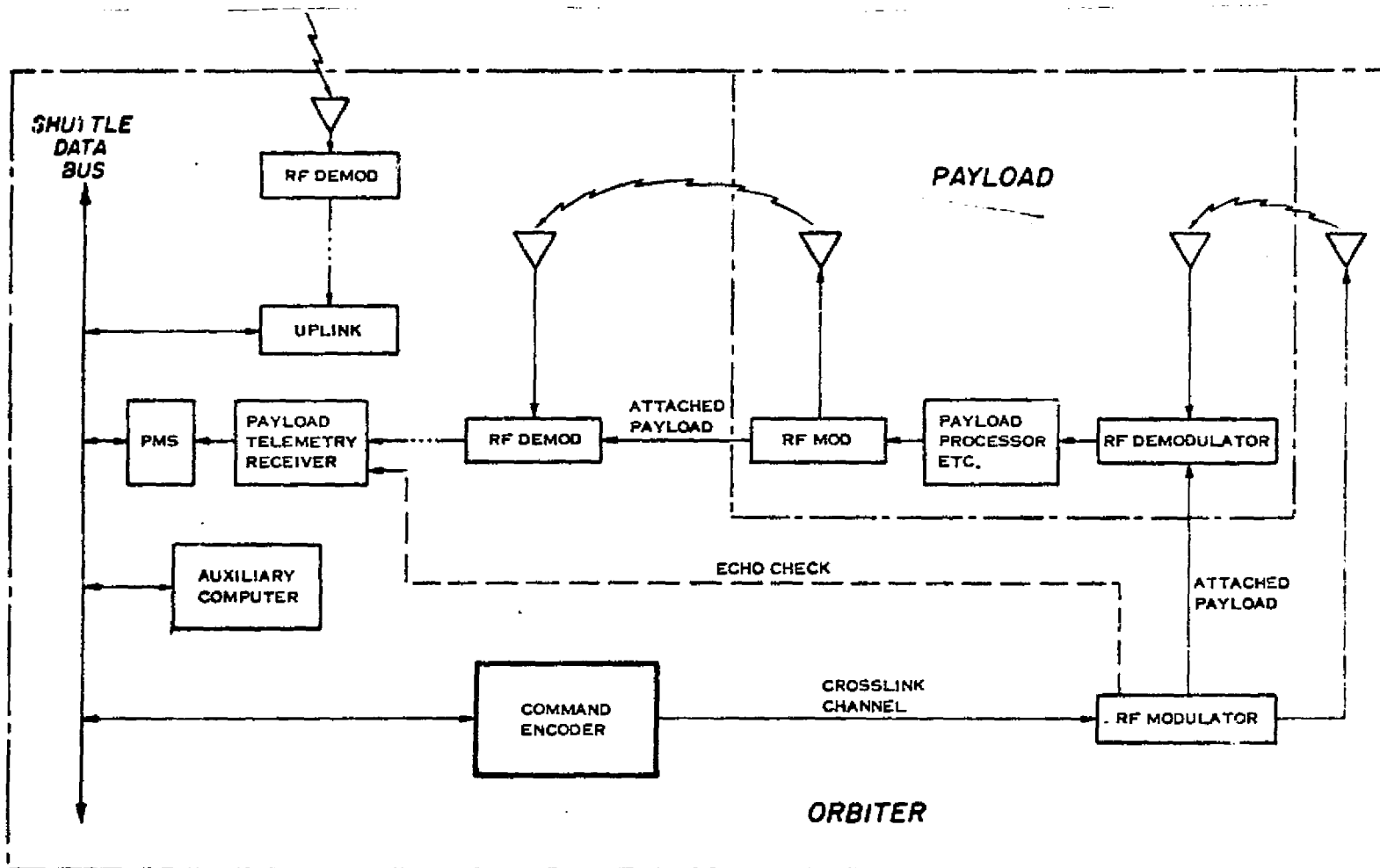


Figure 1-1
Command Encoder System Interfaces

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test set hardware and sytem packaging, respectively. The software required for both the Command Encoder brassboard and test set is described in Section III.

II. COMMAND ENCODER

A. SYSTEM DESIGN

1.0 BASIC CONCEPT

The Command Encoder Design is comprised of two conceptually distinct units - the Coding and Format Generation Unit; and the Modulator Unit (see Figure 1-1). The Coding and Format Generation Unit accepts commands on a priority basis, encodes them, places them in the proper format and passes the encoded data on to the Modulator Unit. In addition, it also:

- a. Keeps track of which messages have been verified and which have not,
- b. retains all information until it has been verified, and
- c. retransmits any information not verified within a specified time.

The Modulator Unit, in turn, appropriately modulates a subcarrier with the encoded data in accordance with the selected payload's input requirements.

The Coding and Format Generation Unit is capable of generating 19 different types (6 NASA and 13 DOD) of commands, and is sufficiently flexible to accommodate new encoding techniques. In addition, NASA1 commands may be time multiplexed with digital voice data, and all DOD commands are passed through the encrypter interface. The Modulator Unit employs five modulation techniques (tone, tone digital, PCM/PSK [NRZ], PCM/PSK [BI-Ø-L] and PCM/FSK) to support anticipated DOD and NASA command system requirements.

A transparent data mode is accepted in all command types except NASA3 and NASA4. When specified, the formatting function of the Command Encoder is bypassed and the command data block contained in the buffer memory is processed exactly as if it were formatted data.

Telemetry validation techniques consist of operator-selectable bit-by-bit validation, acknowledgement and echo checks. This validation information comes back across the Data Bus and when necessary is compared with the transmitted information stored in the Coding and Format Generation Unit.

2.0 COMMAND ENCODER FUNCTIONAL DESCRIPTION

Inputs to the Command Encoder are received from the following sources:

(a) Auxiliary Computer; (b) Performance Monitor System (for verification feedback), (c) operator controls (for manual operation), and (d) delta voice modulator (digital voice). Inputs (a) to (c) utilize a common interface bus under Auxiliary Computer control, while (d) utilizes a separate interface. The only system outputs are a baseband modulated waveform to the crosslink rf system, and status information as requested by the Auxiliary Computer. In addition, an input/output Encrypter interface is provided for DOD missions. Figure 2-1 is a detailed functional block diagram of the Command Encoder.

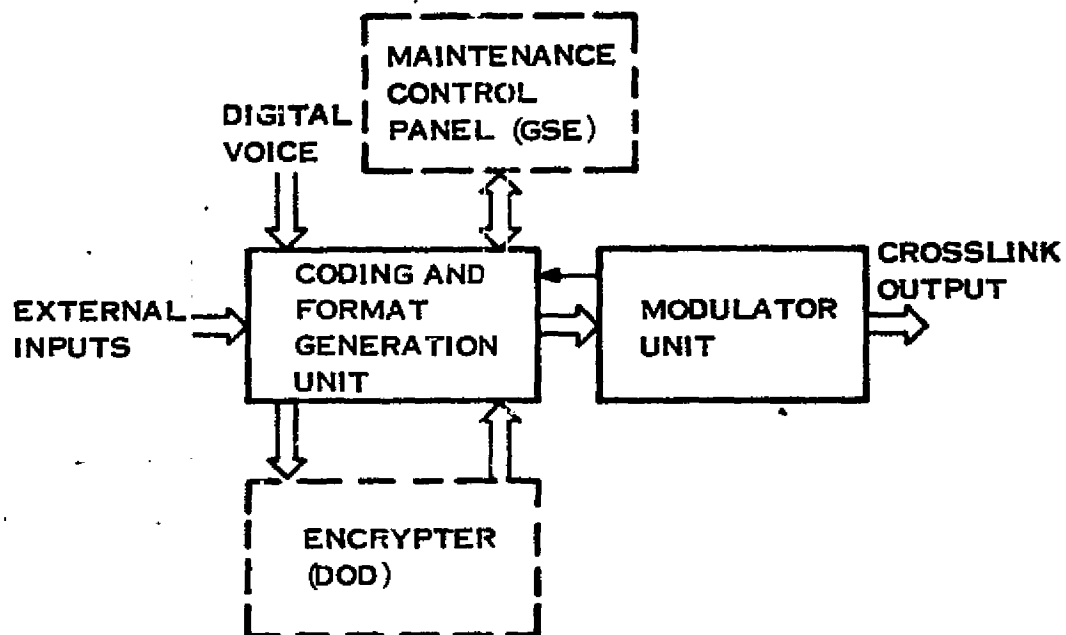


Figure 1-1 - Baseline Block Diagram

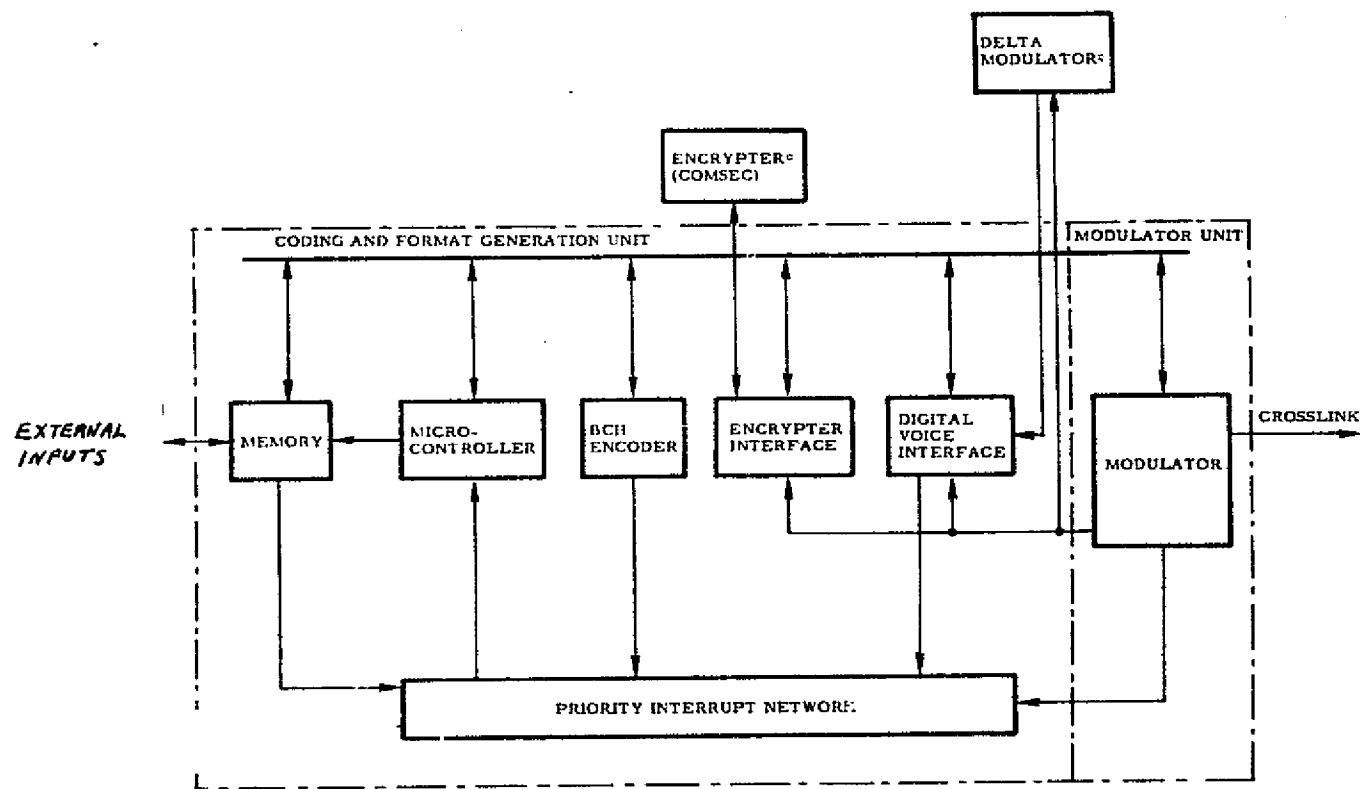


Figure 2-1 Command Encoder Detailed Functional Block Diagram

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2.0 (Command Encoder Functional Description, Continued)

The Coding and Format Generation Unit is comprised of a two-port memory, an off-the-shelf Raytheon Microprocessor, BCH encoder, DOD encrypter and digital voice interfaces, and a priority interrupt network. The two-port memory provides dedicated storage locations for all information transmitted to and from the Auxiliary Computer Simulator, and working storage for the Microprocessor.

The Microprocessor interprets input commands, performs the necessary formatting and encoding, and appropriately drives the multi-mode Modulator Unit. The BCH encoder consists of special purpose hardware to implement the otherwise time-consuming BCH encoding algorithm. The DOD encrypter interface is a full-duplex ternary, serial channel between the Command Encoder and encrypter simulator. The digital voice interface accumulates the 32 KHz serial digital voice information and forms 16 bit words for processing by the Microprocessor. The priority interrupt network minimizes the Microprocessor's response time and facilitates the handling of asynchronous events.

The Modulator Unit is a stand-alone, multi-mode waveform generator which, upon demand from the Microprocessor, digitally synthesizes the crosslink output. The Modulator Unit is treated as a peripheral device to the Microprocessor. It's interface requirements are satisfied by specifying:

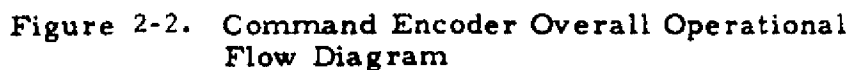
- a. A control word (operational mode, phase shift, etc.)
- b. The subcarrier frequency
- c. The modulation frequency
- d. The symbol time duration

Once transmission is initiated, a modulator interrupt signals any cycle update.

2.1 Functional Operation

A simplified Overall Operational Flow Diagram of the Command Encoder is presented in Figure 2-2. The term Command Channel refers to the path over which command data is presented to the Command Encoder. Regardless of the origin of this data, it is physically transmitted from the Auxiliary Computer (Simulator in the Test Set) over the Data Bus to the Command Encoder. The PMS Channel presents the telemetry feedback information, received by the Performance Monitor System, to the Command Encoder. This information also is transmitted over the Auxiliary Computer Data Bus. All communication over this bus is initiated by the Auxiliary Computer which addresses the desired peripheral device (e.g., the Command Encoder) and indicates the consecutive locations in the device's input memory into which the associated information is to be written, or from which it is to be read onto the bus.

As can be seen from the flow diagram, once the presence of a new command is detected, the Auxiliary Computer first reads the memory location in the Command Encoder containing the status word and if a not-busy condition is indicated, the computer writes appropriate information into the instruction,



2.1 (Functional Operation, Continued)

data block and Command Channel Message locations of the Command Encoder's input memory. Receipt of the Command Channel Message precipitates an Input Interrupt which initiates the processing of the new command by the Coding and Format Generation Unit. The status word is updated by this Unit and the new command information is moved to a working area where the various instruction fields are disassembled and decoded. Then a service routine is entered to initialize the Modulator Unit and transmit the command message block utilizing the appropriate modulation technique. Once the complete block has been transmitted, the Modulator Unit is set-up to time out 30 ms (validation response overdue time).

Meanwhile, when the Auxiliary Computer detects the presence of telemetry feedback, the computer checks the status of the PMS Buffer, writes the telemetry validation information into the input memory, and issues a PMS Channel Message which generates the PMS Interrupt for the Coding and Format Generation Unit. Subsequently, the interrupt causes the Command Encoder to perform the operator-selected validity checks and appropriately update it's status words.

If the command contains more than one data block, the Auxiliary Computer, which periodically checks the Command Channel Status, is now permitted to forward the next data block to the Command Encoder. Again, the Input Interrupt is generated and the Coding and Format Generation Unit assembles the command, serially outputs the command message through the Modulator Unit and awaits the telemetry feedback. This Update Sequence continues until all data blocks have been transmitted or a validity check failure is detected (due to erroneous feedback or no feedback within 30 ms). If so indicated in the Command Instruction, the failed block is retransmitted, and if a "hard-failure" is detected, the command is aborted and the status is updated to indicate the failure.

The presence of higher priority commands within the Auxiliary Computer requires the issuance of an additional "HIPRI" Command Channel Message before the initial sequence is started, in order to affect an orderly abortion of the command presently in progress.

2.2 Test Set Design

The test set permits complete input to output real-time validation of the Command Encoder system performance. The use of hardware identical to that in the Command Encoder and in other Raytheon off-the-shelf equipment minimizes the development cost while still providing system flexibility.

As shown in Figure 2-3, the test set is comprised of an Auxiliary Computer Simulator (Microprocessor), a Command Encoder output interface simulator and a Local Control Panel.

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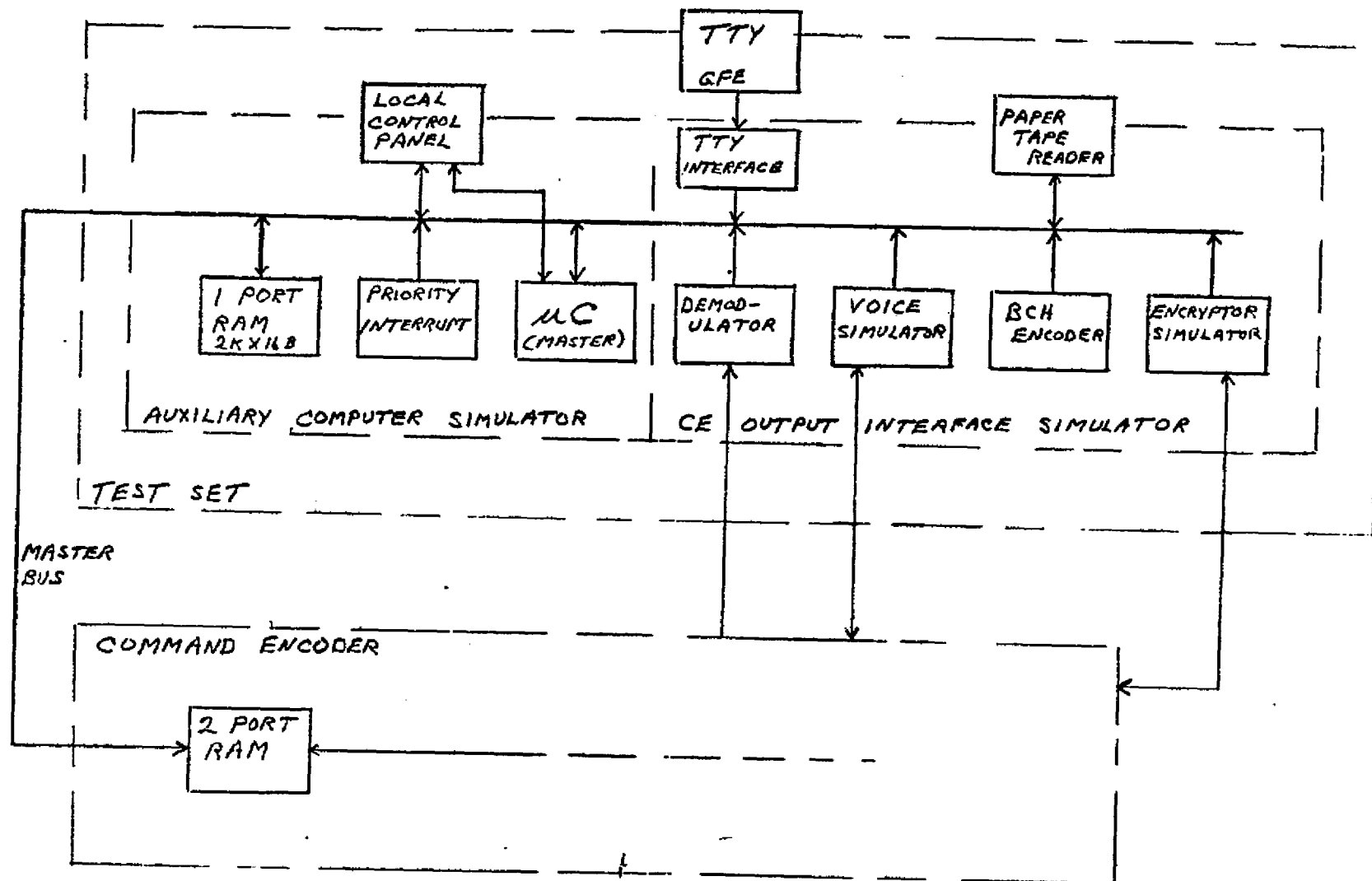


FIG. 2-3 TEST SET BLOCK DIAGRAM

2.2.1 Auxiliary Computer Simulator

The Auxiliary Computer Simulator consists of a Microprocessor identical to that in the Command Encoder, 6K words of semiconductor memory, a paper tape reader, and a TTY interface. The Microprocessor and memory emulate the Auxiliary Computer and the Microprocessor-standard paper tape reader provides a program back-up storage media for the volatile semiconductor memory.

The onboard command encoder serial data bus interface is simulated with the parallel data address and control signals between the test set microprocessor and the command encoder two-port memory.

The Microprocessor generates all the Command Words, Command Instructions, and Command Data Words sent over the data bus to the Command Encoder. The operator can designate the intended payload address and specify the types of verification required, the message block length, priority, number of blocks to be transmitted, the number of retransmissions to be attempted, etc., through the TTY at the beginning of each run. The operator can also specify any one of five modes for generating the actual data to be transmitted: (1) all zeros data; (2) all-ones data; (3) alternating zeros and ones; (4) counting reference data (i.e. the references 00...000, 00...001, 00...010, etc.); and (5) arbitrary patterns entered by operator.

The Microprocessor also simulates the Performance Monitoring Subsystem (PMS) by generating the appropriate message validations. In order to exercise the Command Encoder's retransmission and status generation capability, the operator can designate which message words are not to be properly acknowledged (e.g. the 8th word, the 6th word in each block, or every 10th word). The PMS will then generate an improper acknowledgment (i.e. will insert a bit error in the case of bit-by-bit validation or will otherwise fail to acknowledge the transmitted message within the allotted 30 msec interval).

In addition, the Microprocessor records in specified memory locations pertinent data concerning each run (e.g. Number of message blocks received, last 256 bits received, number of received retransmissions, results of Auxiliary Computer failure analysis, etc.). Any disparity between the received data and that actually anticipated by the Microprocessor at any time during a run causes a program halt, thereby allowing the operator to diagnose the difficulty by reading the appropriate memory locations in both the Auxiliary Computer Simulator and the Command Encoder Microprocessor.

The paper tape reader, Remex RRS7300, is designed to permit the reading of 5, 6, 7 or 8 level perforated tape by the Microprocessor. It can operate under interrupt control (with address vectors to the appropriate interrupt service subroutines), or under program control via the "SKIP" line. Tape read rate is 300 characters per second, and tape handling is via self contained reels.

2.2.2 CE Output Interface Simulator

This interface simulator consists of an encrypter simulator, a digital voice generator, a BCH encoder and a set of baseband demodulators. All but the BCH encoder are unique to the CE test set (the encoder is identical to that in the Command Encoder). These devices are described briefly in the following paragraphs.

Encrypter Simulator

The primary function of the encrypter simulator is to only verify the operation of the interface signals. Accordingly, the interface simply contains logic that, under control of the test set operator, either repeats or inverts the incoming DOD data, and retransmits it back to the CE.

Digital Voice Generator

The digital voice generator enables the Microprocessor to simulate digital voice in the NASAI output data stream and hence compare the received baseband demodulator output with that transmitted. The operator can specify one of three available data patterns: 0101..., 00110011..., and walking bits.

BCH Encoder

An encoder is included in the Test Set to facilitate checking the demodulated BCH encoded NASAI command types. Closed-loop checking of the received NASAI commands requires the regeneration of the appended parity check bits. The information bits (addresses and data) are checked, as they are for all modulation formats, by retaining a copy of the transmitted command instruction and data in the Auxiliary Computer simulator. The 48-bit formatted command is recycled through an encoder and the resultant parity bits compared with those in the transmitted command.

Baseband Demodulators and Demodulator Interface

The baseband demodulators and demodulator interface provide all the necessary demodulation and data formatting for interfacing the Command Encoder Modulator and the CE Test Set Microprocessor. Figure 2-4 illustrates the functional partitioning of the demodulator. The Input Section contains the analog and digital circuits for converting the seven modulation formats to either serial or parallel NRZ data. The Interface section provides the NRZ serial/parallel conversion, sync detection, mode control, and Microprocessor bus interface. This partitioning utilizes existing Microprocessor interface designs and emphasizes mode-sharing logic in the demodulators.

The purpose of the Test Set is to verify that the desired waveforms are being generated, not to measure the performance attainable when each of

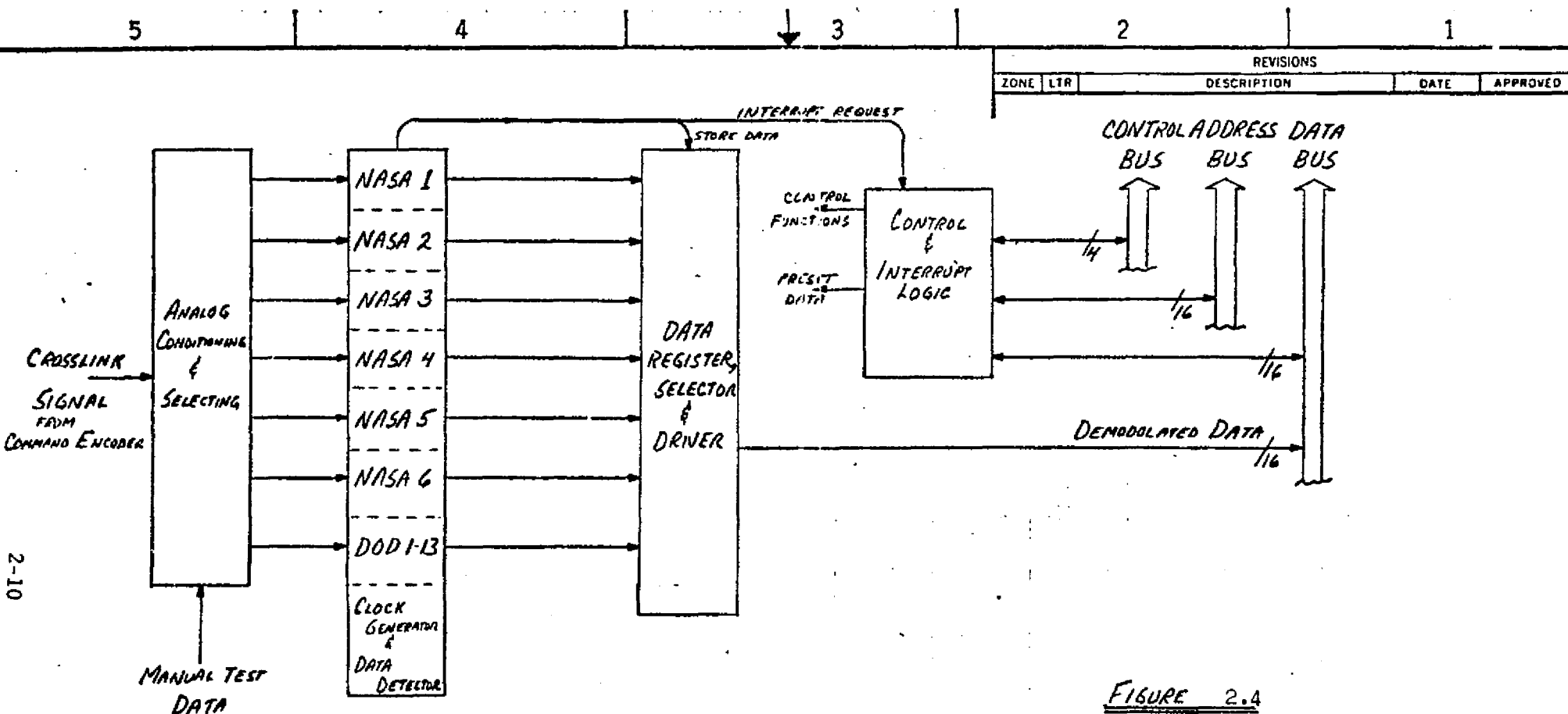


FIGURE 2.4

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QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 1 P. ACE DECIMALS ± 2 P. ACE DECIMALS ± 3 P. ACE DECIMALS ± MATERIAL:			CONTR. NO. DR. <i>11/11/61</i> <i>502/1</i> CHK. APP. <i>11/11/61</i> <i>1002/1</i> D. APPROVED BY DIRECTION OF		
NEXT ASSY USED ON APPLICATION			<div style="text-align: center;"> </div> RAYTHEON COMPANY LEXINGTON, MASS. 02173 DRAWING TITLE <i>COMMAND ENCODER TEST SET DEMODULATOR FUNCTIONAL BLOCK DIAGRAM</i> SIZE B CODE IDENT NO. 49956 DRAWING NO. SCALE SHEET		

(Baseband Demodulators and Demodulator Interface, Continued)

these modulation schemes are used in the presence of noise. Accordingly, the Test Set demodulators are not designed to approximate ideal matched filters; rather they are designed to measure crucial waveform parameters (e.g. zero-crossing and when relevant, amplitude peaks). The resulting demodulators, while decidedly suboptimum so far as noise-rejection is concerned, demodulate the correct information only if the received waveform closely retains its shape.

2.3 Input Message Formats

The original Auxiliary Computer to Input Interface Unit message formats are summarized in Figure 2-5. The data bus message sequence for the transfer of data to the Command Encoder consisted of one Command Word followed by 1 to 32 data words. The CE MEMORY ADDRESS field specified an address in the CE memory which was to be the starting address for the requested transfer.

Communication between the Auxiliary Computer simulator and the CE is over a 16-bit bilateral data bus with addressing provided on a 16-bit unilateral bus. The CE Interface is one port of the two port random access memory. All I/O to the CE two port RAM is indirect, with the specified address containing the starting address. The range of addressable locations is thereby expanded from 511 to the entire CE memory.

Double buffering of data blocks received from the Auxiliary Computer simulator is provided. To affect the buffering within a reasonable time, a buffer swapping approach is used.

2.3.1 CE Command Instruction (CI)

Four sequential memory locations are required for the storage of the 64-bit CE command instructions issued over the onboard command channels. Bits 1-16, 17-32, 33-48, 49-64 utilize bits 1-16 of the first, bits 1-16 of the second, bits 1-16 of the third word, and bits 1-16 of the fourth word, respectively.

2.3.2 CE Data

The Command Instruction specifies a file of data to be processed by the CE. The file is composed of up to 511 blocks (file length = block count).

COMMAND WORD FORMAT

1	3 4	8 9	13 14	22 23	27 28
CMD SYNC	CE ADDRESS	MODE CONTROL FIELD	CE MEMORY ADDRESS	BLOCK LENGTH	PARITY

COMMAND DATA WORD FORMAT

1	3 4	8 9	24 25	26	27	28
DATA SYNC	CE ADDRESS	DATA	PATTERN CHECK			PARITY
			1	0	1	

RESPONSE DATA WORD FORMAT

1	3 4	8 9	24 25	26	27	28
DATA SYNC	CE ADDRESS	DATA	PWR STATUS	VAL BITE		PARITY

Figure 2-3. Summary of Message Formats

1 Command Word (CW)

The Command Word will contain the following information:

Bits	Field Description
1 - 3	Command Sync - Three-bit code for a Command Word Sync.
3 - 8	CE Address - Five-bit code which identifies that the CE must respond to the transmitted Command Word.
9 - 13	Mode Control Field - Five-bit code used for determining the operational mode of the CE as follows: <ul style="list-style-type: none"> 9 - Return Received Command Data Word 10 - Send BITE Status 11 - Master Reset 12 - Transmit/Receive 13 - Address - Identifies when CE Memory Address specifies input/output buffer memory location or the external control register within the Coding and Format Generation Unit.

Bits Field Description

- 14 - 22 CE Memory Address - Nine-bit code that identifies the address of the command encoder memory location. This code also identifies a starting address for a multiple-word data transfer.
- 23 - 27 Block Length - Five-bit code that identifies the number of data words to be transmitted or received. For a non-zero code, the CE will transmit/receive words from/to monotonically increasing addresses starting at the specified CE memory address.

28 Parity - Odd Parity.

2 Command Data Word (CDW)

The Command Data Word will contain the following information:

Bits	Field Description
1 - 3	Data Sync - Three-bit code for a Command Data Word sync.
4 - 8	CE Address - Five-bit code which identifies that CE must accept the transmitted Command Data Word.
9 - 24	Data - Contains the data to be transferred into the CE.
25 - 27	Pattern code for message validity test.
28	Parity - Odd parity.

3 Response Data Word (RDW)

The Response Data Word will contain the following information:

Bits	Field Description
1 - 3	Data Sync - Three-bit code for a Response Data Word sync.
4 - 8	CE Address - Five-bit code which identifies that the CE is responding to the Command Word.
9 - 24	Data - Contains the requested data.
25	Power Status - Indicates the occurrence of a CE power down/power up sequence since the transmission of the last message.
26	Unused
27	Validity (BITE) - Indicates the status of the CE.
28	Parity - Odd parity.

Figure 2-5

Auxiliary Computer - Input Interface Unit

Me ge sma

COMMAND INSTRUCTION (CI) FORMAT

	15	11	7	2	0
WORD 1	VEH ADDR				VALIDATIONS
WORD 2	TRANS CNT				SPECIAL PARAMTRS.
WORD 3	SPARE				BLOCK COUNT
WORD 4	SPARE				

Word 1:

- Bits 15-12 - RECIPIENT VEHICLE ADDRESS
- Bits 11-8 - RECIPIENT VEHICLE SYSTEM ADDRESS
- Bits 7-3 - FORMAT TYPE (See Table 4.1)
- Bits 2-0 - VALIDITY CHECKS - Bits indicating respectively, whether echo check, acknowledgement, and bit-by-bit validation schemes are to be used for command verification (1 = yes, 0 = no).

Word 2:

- Bits 15-12 - TRANSMISSION COUNT - Number of times a record is to be retransmitted by CE upon validation failure.
- Bits 11-8 - RECORD COUNT - Number of records (variable length) per block (max = 16)
- Bit 7 - TRANSPARENT MODE - 1 = transparent, 0 = normal
- Bits 6-0 - SPECIAL PARAMETERS

Word 3:

- Bits 15-9 - SPARES
- Bits 8-0 - BLOCK COUNT - Number of blocks to be transmitted in current sequence.

Word 4:

- Bits 15-0 - SPARES

Each block consists of 1 to 16 records. Each record is composed as dictated by the particular format type (64 bit max.). The two command channel buffers each provide sixty-four memory locations for up to 16 records (one block). The quantity of locations actually used is a function of the Command type. In order to minimize the data bus transmission overhead, all record words are accepted in a modular 16 bit format using sequential memory locations. Figure 2-6 depicts the word packing of "long" and "short" data records.

2.3.3 Command Channel Message

A Command Channel Message memory location is provided for the command channel. Its primary function is to provide synchronization between the Command Encoder and input channels by creating an interrupt each time a message is written into the appropriate location (20g).

COMMAND CHANNEL MESSAGE (CCMSG) WORD

FORMAT

15	14	13	5	0
HI PRI	NCI	NBD	UNUSED	DWC

Bit 15 - HIPRI: Perform an orderly abort of current CI in preparation for a higher priority CI.

Bit 14 - NEW COMMAND INSTRUCTION: The CI input buffer has been filled with a new CI.

Bit 13 - NEW DATA BLOCK: The data block input buffer has been filled with new data.

Bits 12-6 - UNUSED

Bits 5-0 - DATA WORD COUNT: The number of 16-bit words associated with the new data block.

WORD	64W X 16b	
1	DATA WORD 1 BITS 1-16	
2	DATA WORD 1 BITS 17-32	
3	DATA WORD 1 BITS 33-48	
4	DATA WORD 1 BITS 49-57	NOT USED
5	DATA WORD 2 BITS 1-16	
	•	
	•	
	•	
64	DATA WORD 16 BITS 49-57	NOT USED

NASA 5 FORMAT

WORD	64W X 16b	
1	DATA WORD 1	NOT USED
2	DATA WORD 2	NOT USED
	•	
	•	
	•	
16	DATA WORD 16	NOT USED
	NOT USED	
64		

DOD 1 FORMAT

FIGURE 2-6 CE DATA-WORD PACKING

2.3.4 Command Channel Status Word (CCSW)

The following Command Channel Status word is maintained for the CE command channel.

15	14	13	12	11	10	9	8	0
CE BUSY	CI REQST	DB REQST	INV CC MSG	INV CI	WCF	FVER	VERIFIED BLOCK COUNT	

Bit 15 - CE BUSY: Set when the CE accepts a CI and reset when the requested processing is complete.

Bit 14 - CI REQUEST: Set when the CE begins processing the last data block of the previous CI. (Note: This implements double buffering of CI's)

Bit 13 - DATA BLOCK REQUEST: Set when the input data block buffer is empty.

Bit 12 - INVALID COMMAND CHANNEL MESSAGE: Last CC message contained an invalid code or a valid message which is illegal at this time. The invalid message word is saved for possible interrogation by the Auxiliary Computer.

Bit 11 - INVALID COMMAND INSTRUCTION: Last CI contained an invalid code or a valid code illegal at this time.

Bit 10 - WORD COUNT FAILURE: Set when the word count for a data block specified in a CC Message (CCMSG) does not agree with the word count specified in the CI.

Bit 9 - FAILED VERIFICATION: Last block processed failed one or more of the requested validations.

Bit 8-0 - VERIFIED BLOCK COUNT: Number of last block to have passed all requested validations.

2.3.5 Echo Check and Bit-by-Bit Validation

The data fed back through the PMS is utilized to verify proper command transmission. If correct, this data shall be identical to the transmitted command. Hence, ten memory locations are provided to handle the longest output command format (NASA2) from each feedback channel.

Both bit-by-bit and echo validations will be done on an output word basis. It is assumed that PMS data will be returned in Output Command Formats. No validations will be done in Transparent mode.

2.3.6 PMS Channel Status Word

One memory location is utilized to indicate the status of the PMS input.

PMS CHANNEL STATUS WORD

15	14	13	12	11	10	9	8	7	3	2
ECHO	BBB	ACK	ECHO FAIL	BBB FAIL	ACK FAIL	RTF	IPM	SPARES	RE TIME	SPARES

Bit 15 - ECHO Check Buffer Full

Bit 14 - Bit-by-Bit Buffer Full

Bit 13 - ACK Received

Bit 12 - Last Word Failed ECHO Check

Bit 11 - Last Word Failed Bit-by-Bit Validation

Bit 10 - Last Word Failed Acknowledgement

Bit 9 - Last Word Failed 30 MS Response Time Criteria

Bit 8 - Last PMS Channel Message Word was Invalid

Bit 7-3 - SPARES

Bit 2 - Last record transmitted was a retransmit of the previous record.

Bit 1,0 - SPARES

2.3.7 PMS Channel Message

The PMS Channel Message is used to notify the Command Encoder that feedback has been inserted into the PMS Input Buffer and synchronization is provided by generating an interrupt whenever a message is written into memory location 21g.

PMS CHANNEL MESSAGE

15	14	13	12	11	3	0
ECHO	BB	ACK			WORD COUNT	

Bit 15 - ECHO Check Buffer Updated

Bit 14 - Bit-by-Bit Buffer Updated

Bit 13-12 - Acknowledge Verification (11 = Pos, 10 = Negative)

Bit 11-4 - SPARES

Bit 3-0 - WORD COUNT - Number of 16-bit words written into the specified buffer.

2.3.8 Bite Status Word

The CE BITE hardware causes interrupts to the CE microprocessor, as well as external detectors. Upon detection of the fault, the CE will master clear the modulator, set the appropriate bit in the BITE status word and halt.

The address of the BITEGW is 12 (octal 14). The bit assignments are:

BITE STATUS WORD

15	14	13	12	0
HBUS DET	ACT DET	TIMER INT	SPARES	

Bit 15 - Hung Bus State detected

Bit 14 - Activity Detector Fault detected.

Bit 13 - Timer Interrupt Fault

Bits 12-0 - SPARES

2.3.9 Invalid Channel Message Word

Upon detection of an invalid channel message word, the message word will be saved for possible interrogation by the auxiliary computer. The addresses for the Command Channel Invalid Message word and the PMS Channel Invalid Message word are, respectively, 13 and 14.

2.3.10 Computer-Controlled CE Input/Output Handshaking

This section documents the input/output service routine required to drive the command encoder.

The Command Encoder provides buffering for two record blocks (up to 32 input records). Note that two data bus transmissions would be required from the onboard computer to send one block of input records. The maximum data bus transmission is limited to thirty-two 16-bit words, as specified by the data bus command word, while the maximum input record block size, as specified in the CI, is sixteen 64-bit words. Two current DB buffer pointers are provided to facilitate handling of the two separate data bus transmission from the onboard computer. The future addition of an Input Handler Unit and a Data Bus Interface Adapter would allow Command Encoder operation with an Auxiliary Computer via a serial data bus. When the presence of a new command is detected, the Auxiliary Computer first reads the memory location in the CE containing the status word (CCSW). If the Command Instruction (CI) request bit and the Data Block (DB) request bit are set, the computer writes appropriate information into the instruction, data block and Command Channel Message (CCMSG) location of the CE's input memory. Receipt of

2.3.10 (Computer-Controlled CE Input/Output Handshaking, Continued)

the CCMSG precipitates an Input Interrupt which initiates the processing of the new command by the Coding and Format Generation Unit (CFG). This unit buffers the input data block and updates the CCSW to indicate that a new DB can be transmitted. The command instruction is decoded, and the modulator unit is set to start the initialization sequence. The modulator's data request interrupt is serviced until a command word is completed, at which time the interval timer is set for 30 ms (validation response overdue time).

When the auxiliary computer detects the presence of validation data, it checks the Performance Monitor System Channel Status Word (PMSSW), transfers data to the appropriate input memory buffer, and issues a PMS Channel Message (PMSMSG). Receipt of the PMSMSG generates the PMS Interrupt causing the CE to perform the requested validity checks and update the PMSSW.

The above sequence is repeated for each command word until the DB is complete. The cycle is resumed with the next DB and continues until the last DB is complete.

The presence of higher priority commands within the Auxiliary Computer requires the issuance of an additional "HIPRI" CCMSG to effect an orderly abortion of the command presently in progress.

2.4 Output Command Formats

The CE is capable of generating payload link commands in nineteen different format types, or in a transparent mode where the commands are transmitted as received.

Information regarding the message is extracted from the Instruction word such as: word count, block count, command type, etc. The first output command is formatted and stored in a "temporary" area from which it is later transferred to a dedicated "output command" buffer area. In the case of NASA 1 and DOD commands, additional encoding or encryption is performed. The formatted output commands are then transferred to the modulator unit. Following is a description of each format type. (The formats are illustrated in Appendix C).

2.4.1 NASA 1 (Encoded BI-0-L)

1 - 4	5 - 8	9 - 48	19 - 128
vehicle	system	data	parity bits
address	address		

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2.4.2 NASA 2 (Apollo)

1 - 3	4 - 6	7 - n
vehicle address	system address	data (n = 12,22,27 or 32)

(N.B. each "zero" vehicle address bit in this format is represented by a 5-bit pattern A and each "one" vehicle address bit by \bar{A} ; similarly, each "zero" system address and data bit is represented by 5-bit pattern B, and each "one" by \bar{B}).

2.4.3 NASA 3 (Tone Standard)

1 - 4	5 - 7	8 - 10	11 - 13
address (0000 not used)	executive word (up to 3 3-bit bytes; 000 not used)		

2.4.4 NASA 4 (Tone Digital Standard)

1 - 8	9 - 16	17 - 24	25 - 32	33 - 40
address (all addresses contain either 2 or 6 "zeros")	address (repeated)	execute word (all execute words con- tain 4 "zeros" and 4 "ones")	execute word (repeated)	execute word (repeated)

2.4.5 NASA 5 (PCM/FSK Standard)

1 - 7	8 - n
address	command ($7 \leq n \leq 64$; n fixed for any given spacecraft)

(Note: Memory load format accommodated by specifying number of words constituting the total message; only the first word contains the address).

2.4.6 DOD 1. 7-Bit Command

1	2 - 3	4 - 7
parity	address	command function

2.4.7 DOD 2. 14-Bit Command

1 - 5	6 - 13	14
address	command function	odd parity

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2.4.8 DOD 3. 15-Bit Command

1 - 3	4 - 12	13 - 14	15
address	command function	constant bits (all commands)	parity

2.4.9 DOD 4. 16-Bit Command

1 - 5	6 - 13	14	15 - 16
address	command byte	odd parity	fill

2.4.10 DOD 5

1 - 5	6 - 8	9 - 19	20
system address	subsystem address	command function	odd parity

2.4.11 DOD 6. 25-Bit Command

1 - 4	5 - 9	10	11 - 18	19 - 24	25
system address	command mode	even parity on bits 1 - 9	variable command data	subsystem address	even parity on bits 11 - 2

2.4.12 DOD 7

1 - 5	6 - 8	9 - 16	17 - 26	27
address	magnitude function	discrete command	magnitude function	parity

2.4.13 DOD 8

1	2 - 7	8 - 13	14 - 19	20 - 25	26 - 3
sync bit	address	command supplement	command	command supplement	command

2.4.14 DOD 9. 35-Bit Command

1 - 5	6 - 35
address	command function

2.4.15 DOD 10. 39-Bit Command

1 - 22	23	24 - 38	39
vehicle time code	parity on bits 1 - 22	command function	parity

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2.4.16 DOD 11. 47-Bit Command

1 - 3	4 - 13	14 - 25	26 - 45	46	47
address	memory location address	command function	time table	parity on bits 1 - 25	overall parity

2.4.17 DOD 12. 63-Bit Command

1 - 21	22 - 42	43	44 - 63
fixed command count	variable command count	fill bit	command data

2.4.18 DOD 13. 64-Bit Command

1 - 32	33	34 - 37	38 - 41	42 - 50	51 - 59	60 - 64
pre- amble	sync bit	address supplement	address	command supplement	command	timing

2.5 Output Formatting Definition

This section defines the output command buildup from the command instruction contents.

2.5.1 NASA1 and NASA6

Output Record Bits

From

0-2	Set to zero
3-6	Bits 15-12 of CI Word 1
7-10	Bits 11-8 of CI Word 1
11-50	Input Data
51-128	BCH Encoder

2.5.2 NASA2

Data length (6,16,21,26 bits) in special parameter field of command instruction. For transparent mode, the data length cannot exceed 127 bits.

Output Record Bits

From

1-15	Formatted from bits 14-12 of CI Word 1
16-30	Formatted from bits 10-8 of CI Word 1
31 - End	Formatted from data

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The 5-bit "A" and "B" patterns will be:

A0	00101	A11	01011	B0	10000	B11	11011
A1	00001	A12	10011	B1	10001	B12	11100
A2	00010	A13	10010	B2	10010	B13	11101
A3	00011	A14	10001	B3	10011	B14	11110
A4	11011	A15	10000	B4	10100	B15	00100
A5	11010			B5	10101		
A6	11001			B6	10110		
A7	11000			B7	10111		
A8	01000			B8	11000		
A9	01001			B9	11001		
A10	01000			B10	11010		

2.5.3 NASA 3

Output Record Bits

1-4
5 - End

From

Bits 11-8 of CI Word 1
Input data

2.5.4 NASA 4

Output Record Bits

1-8
9-16
17-24
25-32
33-40

From

Bits 15-8 of CI Word 1
Bits 15-8 of CI Word 1
Input data
Same data
Same data

2.5.5 NASA 5

Total output word length (input record length) plus 7 will be in the special parameters field of the CI.

Output Record Bits

1-7
8 - End

From

Bits 14-8 of CI Word 1
Input data

2.5.6 DOD 1

Output Record Bits

1
2-3
4-7

even parity on entire word
come from bits 9-8 of CI Word 1
data

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2.5.7 DOD 2

Output Record Bits

1-5	come from bits 12-8 of CI Word 1
6-13	data
14	odd parity on entire word

2.5.8 DOD 3

Output Record Bits

1-3	come from bits 10-8 of CI Word 1
4-12	data
13-14	will be 1's
15	even parity on entire record

2.5.9 DOD 4

Output Record Bits

1-5	come from bits 12-8 of CI Word 1
6-13	data
14	odd parity on bits 1-13
15-16	will be 1's

2.5.10 DOD 5

Output Record Bits

1-8	come from bits 15-8 of CI Word 1
9-19	data
20	odd parity on entire record

2.5.11 DOD 6

Output Record Bits

1-4	come from bits 15-12 of CI Word 1
5-9	data
10	even parity on bits 1-9
11-18	data
19-22	come from bits 11-8 of CI Word 1
23-24	come from special parameters field of CI
25	even parity on bits 11-24

2.5.12 DOD 7

Output Record Bits

1-5	come from bits 12-8 of CI Word 1
6-26	data
27	odd parity on entire record

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2.5.13 DOD 8

Output Record Bits

1
2-7
8-31

will be a 1
come from bits 13-8 of CI Word 1
data

2.5.14 DOD 9

Output Record Bits

1-5
6-35

come from bits 12-8 of CI Word 1
data

2.5.15 DOD 10

Output Record Bits

1-22
23
24-38
39

data
even parity on bits 1-22
data
even parity on entire record

2.5.16 DOD 11

Output Record Bits

1-3
4-45
46
47

come from bits 10-8 of CI Word 1
data
even parity on bits 1-25
even parity on entire record

2.5.17 DOD 12

Output Record Bits

1-42
43
44-63

data
will be 1
data

2.5.18 DOD 13

Output Record Bits

1-32
33
34-37
38-41
42-64

will be all 1's
will be 1
1's complement of bits 11-8 of CI Word 1
come from bits 11-8 of CI Word 1
data

2.6 Transparent Transmission

The CE is capable of outputting the command data contained in the CDW (command data word) bypassing the formatting function of the CE for all transmission types except NASA 3 and 4. The command data is output at a continuous bits without the insertion of spacing intervals or deletion of data. The command data sequence is processed by the modulator section of the CE exactly as if it were formatted data. Transparent mode (i.e. no formatting or encoding) leads to new definitions of some types of input. These are specified below:

2.6.1 NASA1, NASA6

If the transparent mode bit is set in a NASA1 or NASA6 CI, the record count is interpreted as the number of continuous 160-bit records in the DB. (Note: The record count field of the CI starts at zero. Zero indicates one record).

2.6.2 NASA2, DOD

In the transparent mode, the TYPE code for DOD's is meaningless. Any DOD TYPE in transparent mode will cause the special parameters field to be interpreted as the word length. The record count is interpreted as the number of specified length records in the buffer. The record length must be a multiple of 16-bits. The above is also true for NASA2.

2.7 Modulator Requirements

2.7.1 Output Performance Specification

- a. The subcarrier frequency satisfies the following requirements:

Selection Resolution	1 Hz
Accuracy	$\pm 0.005\%$
Range	1 to 35 kHz
Total Harmonic Distortion	5%
- b. The modulation frequency satisfies the following requirements:

Selection Resolution	1 Hz
Accuracy	$\pm 0.005\%$
Range	1 to 65,535 Hz
Phase Shift	0 to 7/8 Cycle
Phase Resolution	1/8 Cycle
Waveforms	Sine, Triangle
- c. The modulation feedthrough shall be less than -26 db referenced to the subcarrier.
- d. The modulation shift time shall be less than 1 sec.

2.7.2 Modulation Techniques

NASA 1 (Figure 2-7)

PCM/BI- ϕ -L, 8 kB/sec. (8.066 kB/sec.). Each 128-bit command word is divided into four 32-bit segments and preceded by a 32-bit frame-sync sequence. When time-multiplexed with digital voice, 128 bits of delta modulated voice data is inserted between every 32 bits of command data; the combined information rate is 40kB/sec. (40.330 kB/sec.). Transmission is initiated with a 1 sec. sequence of "ones" in order to establish bit sync. Transmission continues until "stop" instruction received; if no command data available a "null" command is transmitted during that interval.

NASA 2 (Figure 2-8)

A 2 kHz subcarrier is 100 percent phase-modulated by the 1 kB/sec. PCM-PSK data and summed with an equal-amplitude 1 kHz tone. Each transmission is initiated with a 1 sec. sequence of "ones" in order to establish bit sync. Multiples of five zeros are inserted between command blocks when no data is available. The composite PCM-PSK and summed reference frequency modulates a 70 kHz oscillator with a deviation of ± 5 kHz.

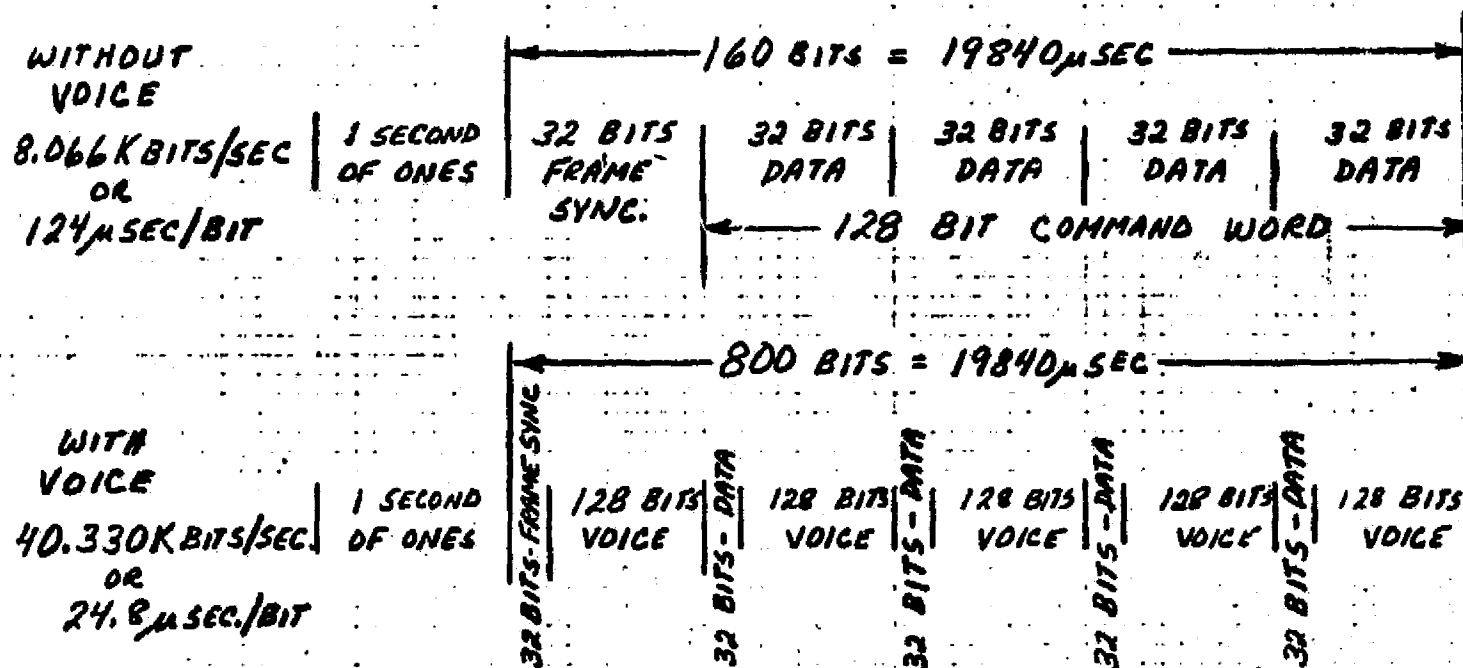
NASA 3 (Figure 2-9)

FSK using up to 15 address tones and seven execute tones as follows:

<u>Address Frequency (Hz)</u>	<u>Execute Frequency (Hz)</u>
1025	2000
1097	2270
1174	2650
1262	3000
1352	3305
1447	3621
1549	3850
1750	
1860	
4245	
4550	
5155	
5451	
5790	
6177	

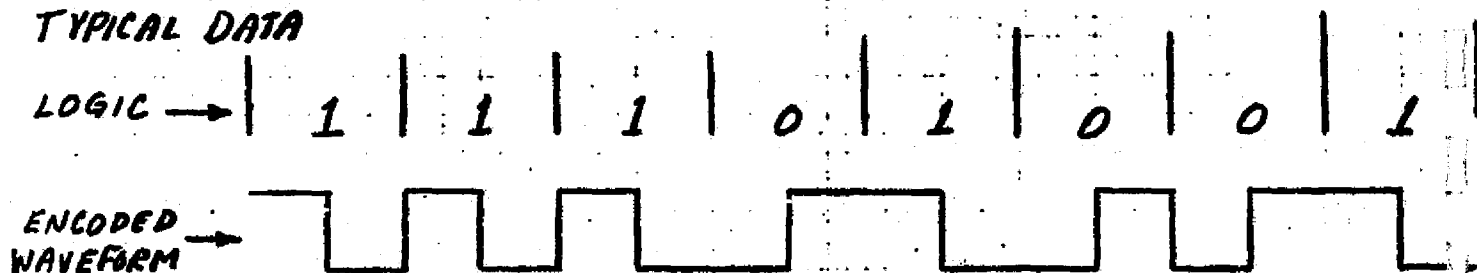
The duration of each tone is equal to 0.5 seconds with an integer in the range $1 \leq l \leq 7$; is specified by bits 29-31 of CE Command Instruction Format. The interval between tones equals 0.5 seconds, and the interval between messages is at least 0.5 seconds.

NASA 1 MESSAGE FORMAT



ENCODED WAVEFORM IS GENERATED BY MULTIPLYING SQUAREWAVE SUB CARRIER DURING EACH BIT TIME BY +1 (NO CHANGE) FOR A LOGIC ONE . OR BY -1 (180° INVERSION) FOR A LOGIC ZERO. 1 BIT TIME = PERIOD OF SQUAREWAVE

TYPICAL DATA



BIT TIME

24.8 μ SEC - WITH VOICE

124 μ SEC - WITHOUT VOICE

$$\frac{\text{BIT TIME INTERVAL}}{\text{SUB CARRIER PERIOD}} = 1$$

FIGURE 2 - 7

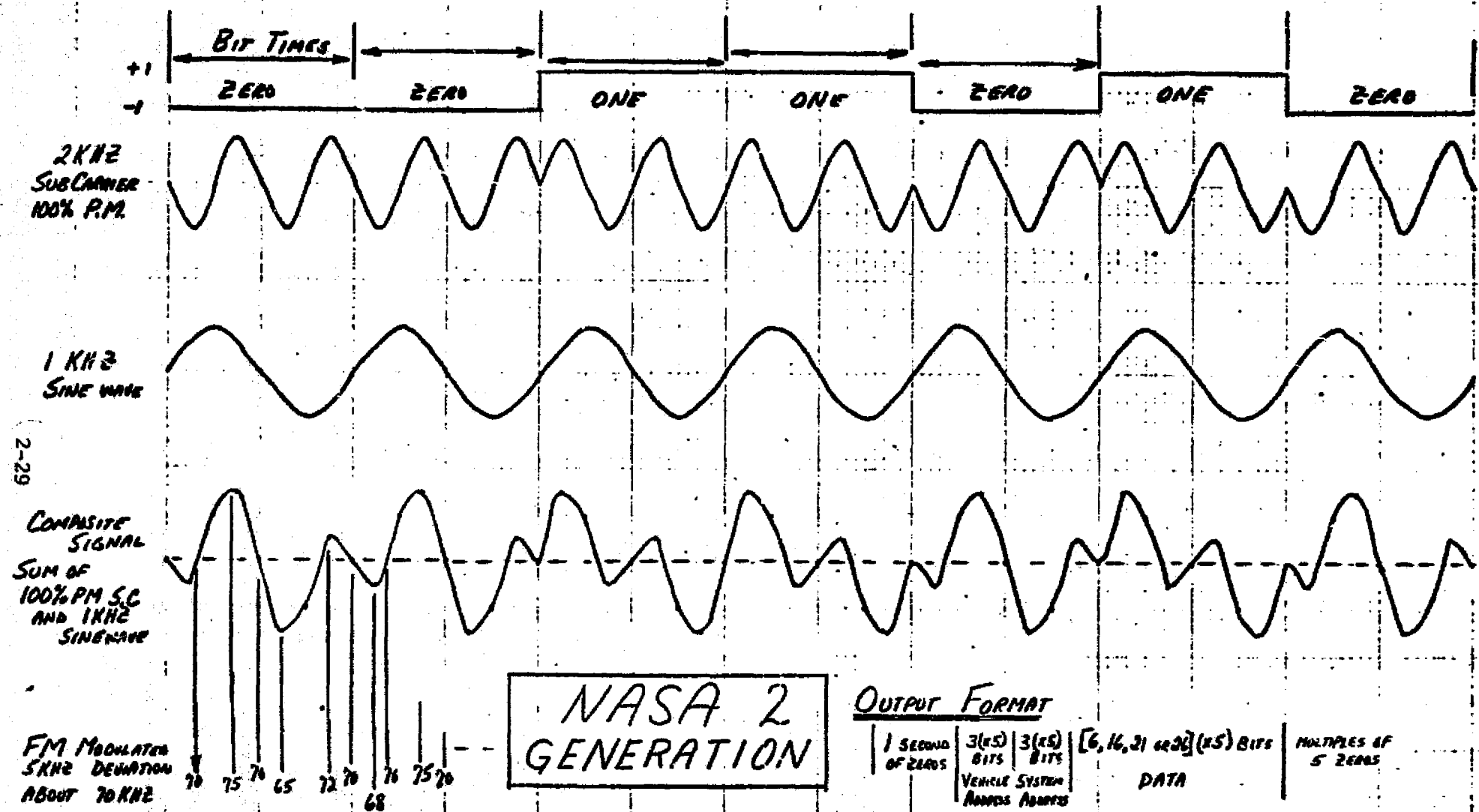
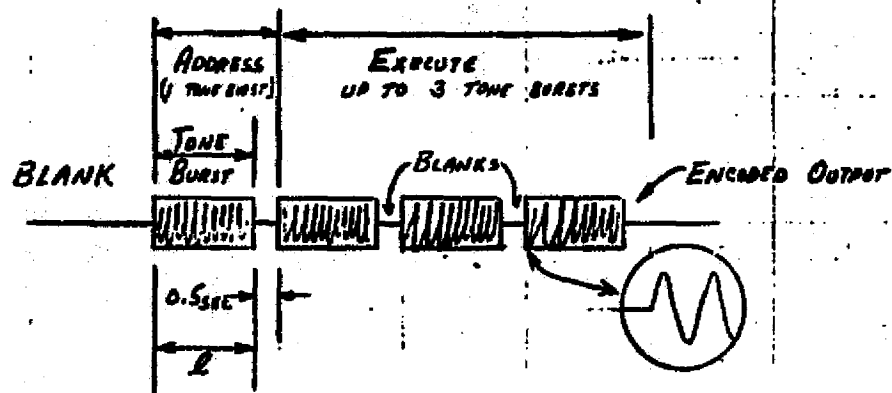


FIGURE 2 - 8

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NASA 3 MESSAGE FORMAT



4 BITS (0000 NOT USED) DETERMINE WHICH OF 15 ADDRESS TONES IS GENERATED
 3 BITS (000 NOT USED) DETERMINES EXECUTE TONE

TURN ON, TURN OFF AND SELECTION OF TONE TO BE A CONTROLLER FUNCTION

DURATION OF BLANK (I.E. NO SIGNAL) = 0.5 SEC. (CONSTANT)

DURATION OF TONE BURST = L. WHERE L = 0.5, 1.0, 1.5, 2.0, 2.5, 3.0 OR 3.5 SEC (IS SPECIFIED IN BITS 29-31 OF CE COMMAND INSTRUCTION)

ADDRESS CONSISTS OF 1 BURST OF

ONE OF THE FOLLOWING FREQUENCIES:

1035	H ₂
1097	
1174	
1262	
1352	
1447	
1549	
1750	
1860	
4250	
4550	
5155	
5451	
5700	
6177	H ₂

EXECUTE CONSISTS OF UP TO 3 TONE BURSTS OF THE FOLLOWING FREQUENCIES

2000	H ₂
2270	
2650	
3000	
3305	
3621	
3860	H ₂

FIGURE 2 - 9

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NASA 4 (Figure 2-10)

Four-symbol pulse duration modulation: 75%, 50%, 25% and 0% (representing "sync", "one", "zero", and "blank", respectively). The subcarrier shall be a fixed tone in the 7000 to 11,024 Hz range. The (100%) pulse interval is defined as 72 subcarrier cycles. Each address word and each execute word is preceded by a "sync" pulse which is in turn preceded by a "blank" pulse. An additional "blank" and "sync" pulse is inserted at the end of transmission.

NASA 5 (Figure 2-11)

Two-tone (using two assigned frequencies in the 7 to 21 KHz band FSK modulated by the PCM-NRZ data. This modulated signal is 50% amplitude modulated by a sinusoidal bit synchronization signal having a period equal to one bit interval. The positive-going zero-crossing of this sync signal is specified to occur either at the beginning of each bit interval, or delayed relative to this point by either 1/4 or 1/2 of the bit interval, or delayed relative to this point by either 1/4 or 1/2 of the bit interval. Allowable bit rates (fixed for each recipient vehicle) in bits/sec: 2^i (i is an integer $3 \leq i \leq 10$) and $100i$ (i an integer $1 \leq i \leq 12$).

Each transmission is initialized by a sequence of 13 (or more) "zeros" followed by a "one" and is terminated by a sequence of (at least) 20 zeros.

NASA 6 (Figure 2-12)

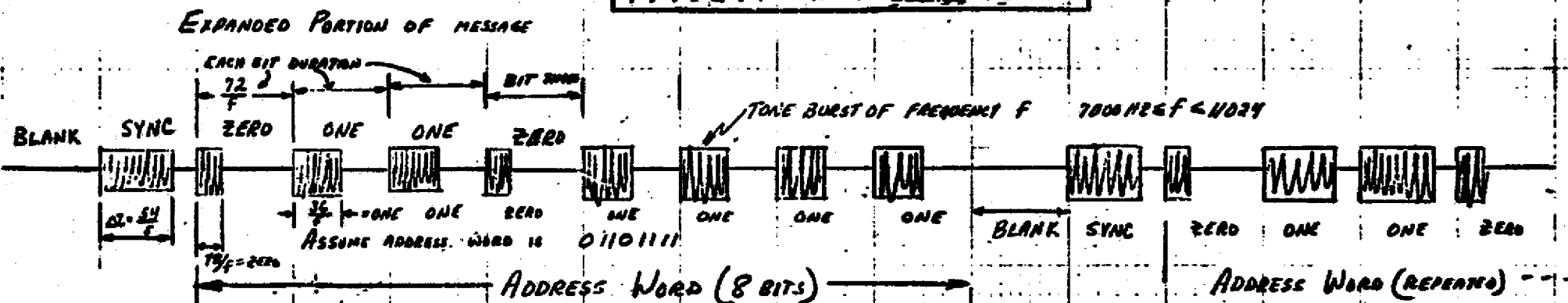
Square wave PSK subcarrier with coherent modulation by PCM-NRZ data. The subcarrier frequency is 2^i Hz, with $i = 1$ to 12. The data rate is 2^j Hz with $j = 0$ to 11. The subcarrier to data ratio is from 2 to 2048.

DOD 1 - 13 (Figure 2 - 13)

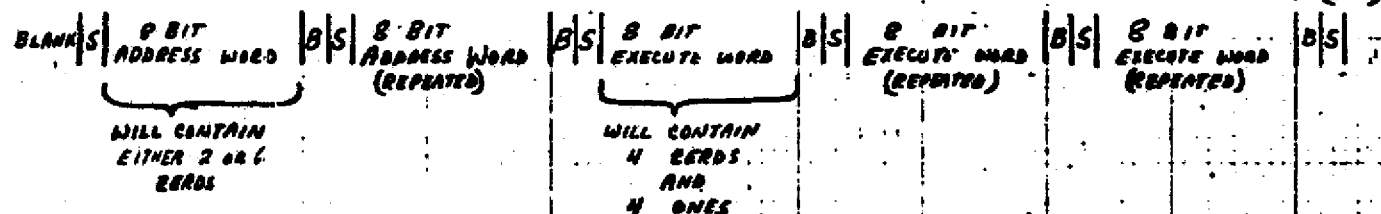
The three-tone FSK modulated by the PCM-NRZ data is either 1 kB/sec or 2 kB/sec. The three tones are 95 kHz ("one"), 76 kHz ("zero"), 65 kHz ("S"). The "S" or space symbol is used only when neither a "one" or a "zero" are available for transmission. The FSK signal is 50% AM modulated by a symmetric triangular wave having a period equal to two bit intervals. The positive-going zero-crossing of the triangular wave is delayed from the bit-transition point by 6/10th of a bit interval.

Each transmission is initialized by a 1-second interval of "S's" and "S's" are inserted between commands when no data is available.

NASA 4 MESSAGE FORMAT



COMPLETE MESSAGE IS AS FOLLOWS: B=BLANK, S=SYNC.



Summary:

A.4 POSSIBLE SYMBOLS TRANSMITTED

1. BLANK - NO SIGNAL
2. SYNC - 54 CYCLES OF SUB CARRIER
3. ONE - 36 CYCLES OF SUB CARRIER
4. ZERO - 18 CYCLES OF SUB CARRIER

TIME DURATION OF PULSE AND BLANKS.
CONTROLLED BY M & N REGISTERS IN
MODULATOR

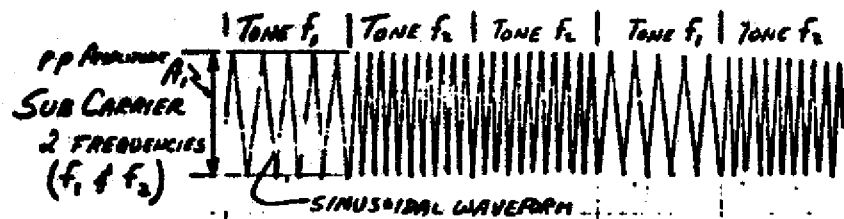
B. Frequency of SOB CANNOT FIRED IN RANGE FROM 7000 Hz TO 11034 Hz

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FIGURE 2 - 10

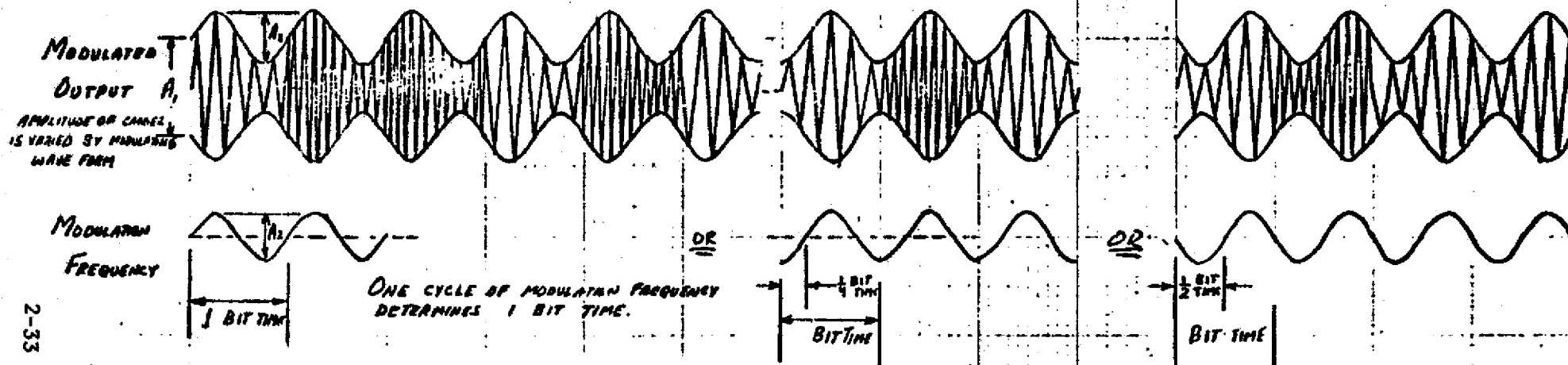


TONE f_1 CORRESPONDS TO A LOGIC 0
TONE f_2 CORRESPONDS TO A LOGIC 1

TWO TONES ASSIGNED
IN RANGE FROM 7KHZ TO 21KHZ

LOGIC STATE TRANSMITTED → 0 1 1 0 1 0 0 1 0 0 0 1 0 0

FOR 50% AMPLITUDE MODULATION, A_2 AMPLITUDE (MODULATION AMPLITUDE) = 0.5 A_1 AMPLITUDE (SUBCARRIER AMPLITUDE)



DELAY OF POSITIVE GOING, ZERO CROSSOVER OF MODULATION FREQUENCY
WITH RESPECT TO BIT TIME MAY BE 0 (COINCIDENT), $\frac{1}{4}$ BIT TIME OR
 $\frac{1}{2}$ BIT TIME. THIS WILL BE FIXED FOR ANY GIVEN VEHICLE (SYSTEM).

MODULATION FREQUENCIES ALLOWABLE (FIXED FOR EACH PARTICULAR SYSTEM)

ARE 2^{λ} BITS/SEC WHERE λ IS AN INTEGER $3 \leq \lambda \leq 10$
AND 100λ BITS/SEC WHERE λ IS AN INTEGER $1 \leq \lambda \leq 12$

COMPLETE NASA 5 COMMAND FORMAT

INITIALIZATION	MESSAGE	TERMINATION
≥ 13 ZEROS	1 ONE 7 BITS ADDRESS	8 - n COMMAND ≥ 20 ZEROS

WHERE n IS AN INTEGER $7 \leq n \leq 64$
BUT IS FIXED FOR ANY PARTICULAR SYSTEM

NASA 5
MESSAGE FORMAT

FIGURE 2 - 11

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NASA 6 (GENERALIZED NASA 1)

in NASA 1 (BI-φ-L), $\frac{\text{BIT TIME}}{\text{PERIOD OF SUB CARRIER}} = 2^0 = 1$

in NASA 6:

$$2^1 \leq \frac{\text{BIT TIME}}{\text{PERIOD OF SUB CARRIER}} \leq 2^4 (2048)$$

$$2^1 \leq \text{FREQUENCY OF SUB CARRIER (SQ. WAVE.)} \leq 2^{12} (4096 \text{ Hz})$$

$$2^0 \leq \text{FREQUENCY OF DATA BITS} \leq 2^4 (2048 \text{ Hz})$$

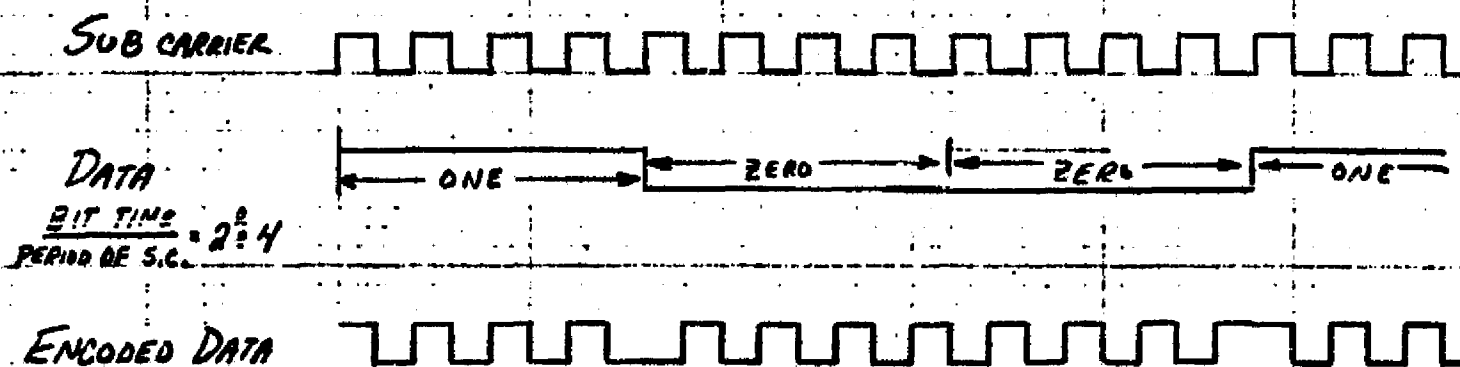


FIGURE 2 - 12

SPACE FREQUENCY = 65 KHZ
 ZERO FREQUENCY = 76 KHZ
 ONE FREQUENCY = 95 KHZ

FREQUENCY OF SUB CARRIER VARIES WITH DESIRED LOGIC STATE (3)

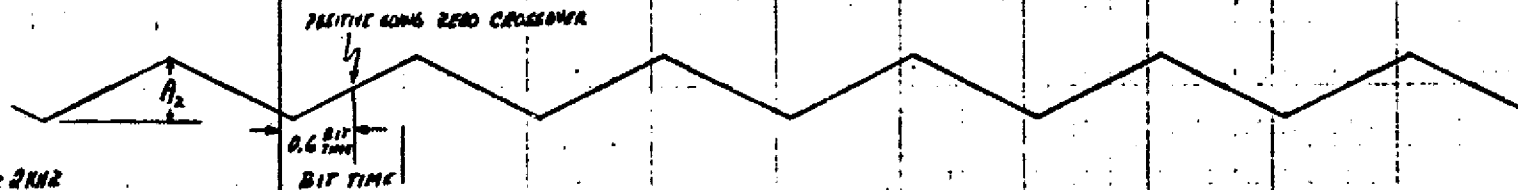


LOGIC STATES

SPACE SPACE SPACE SPACE SPACE ONE ZERO ONE SPACE ZERO SPACE ONE

TRIANGULAR MODULATION FREQUENCY

EITHER 1 KHZ OR 2 KHZ

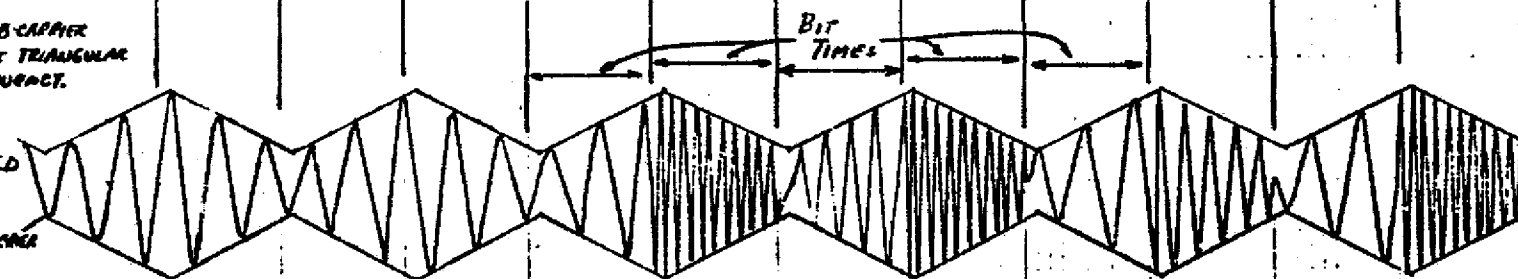


FOR 50% AMPLITUDE MODULATION, A_2 AMPLITUDE = 0.5 A_1 AMPLITUDE

AMPLITUDE OF SUB-CARRIER IS VARIED BY THE TRIANGULAR MODULATION FREQUENCY.

MODULATED OUTPUT

SUM OF SUB-CARRIER AND TRIANGLE MODULATION FREQUENCIES



DOD 1-13
 GENERATION

FIGURE 2 - 13

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2.7.3 Acknowledgement Overdue Time

The worst case response time is 30 milliseconds. If all command-selected validations have not been returned within the response time, the message is retransmitted if the transmission counter is not zero. If zero, the failed validity check is so identified in the Command Channel Status Word.

2.8 Interface Specifications

The CE external interfaces are shown on the CE Test Configuration block diagram, Figure 2-14. Specifications for each interface are listed in the following:

- 2.8.1 Data Bus: A 16-bit tri-state bus with most significant bit (MSB) named MBD15- and least significant bit (LSB) MBD00-
Logic "0" = 2 to 5 VDC
Logic "1" = 0 to 0.8 VDC
- 2.8.2 Address Bus: A 16-bit tri-state bus with MSB named MBA15- and LSB named MBA00-
Logic "0" = 2 to 5 VDC
Logic "1" = 0 to 0.8 VDC
- 2.8.3 Control Bus: Consists of three control lines for Master Bus Request (MBRQE-), Master Bus Acknowledge (MBAK-), and Master Bus Write/Read (MBWRT-).
Logic "0" = 2 to 5 VDC
Logic "1" = 0 to 0.8 VDC
- 2.8.4 Encrypter Interface: Differential TTL-level line drivers and receivers are used on the seven encrypter interface signals. The interface cabling consists of seven twisted-pair lines with an overall shield. Output signals are 1-0-S data out and one clock. Input signals are 1-0-S data-in.
Signal amplitude:
 - logic "0" = 0.0 volts \pm 0.5 volts
 - logic "1" = 5.0 volts \pm 1.0 volts

2.8.5 Digital Voice Modulator

The Command Encoder's digital voice interface consists of a serial input data port and a gated output clock for synchronization. When the modulator is set up for digital voice multiplexing, the 32 KHz square wave clock is enabled and sent out to the digital voice modulator. The leading edge is to be used by the modulator to update its output data and the trailing edge is used as a strobe within the Coding and Format Generation Unit's digital voice buffer (See Figure 2 - 15).

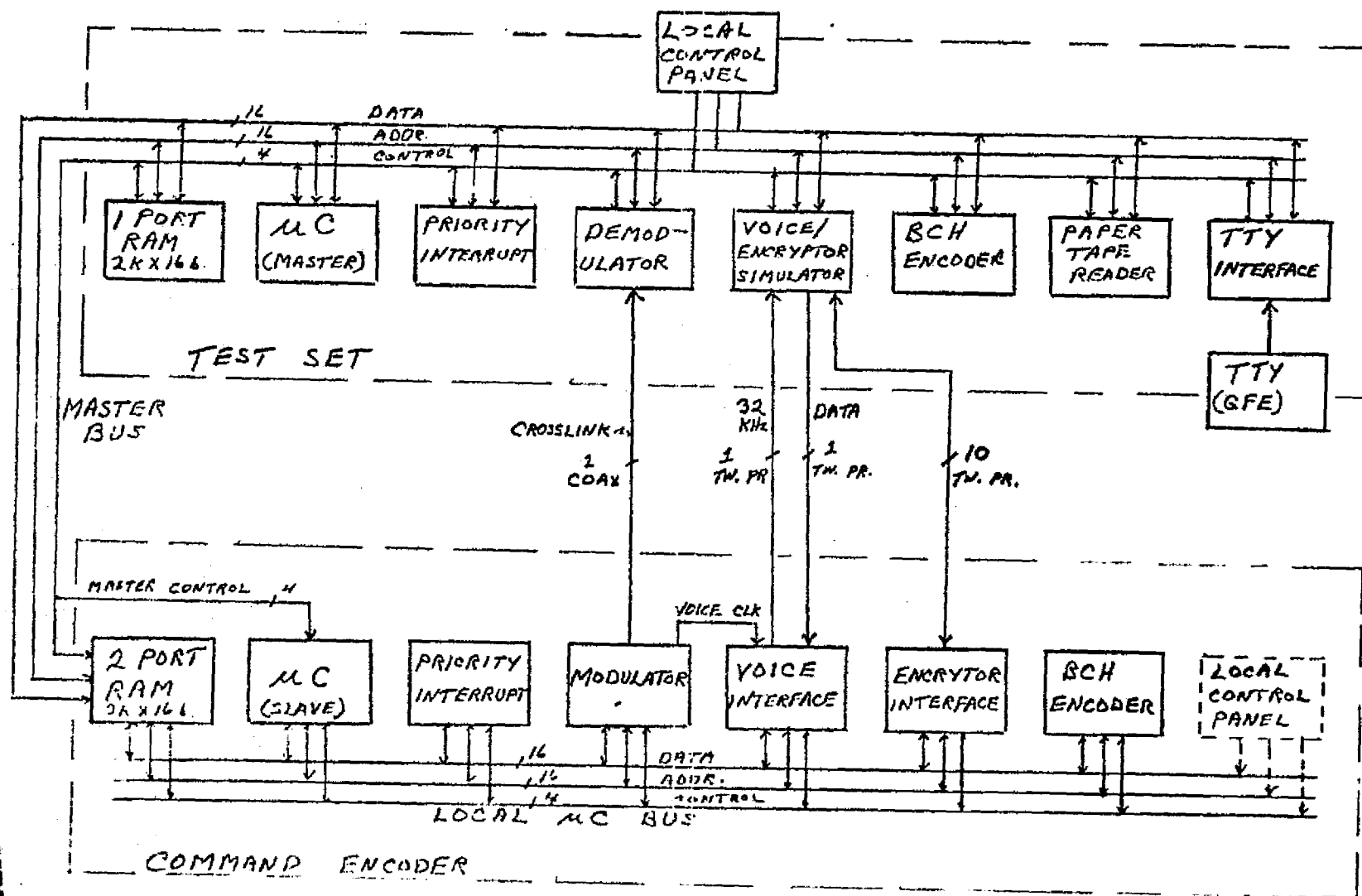


FIG. 2-14 COMMAND ENCODER TEST CONFIGURATION

2.8.5 (Digital Voice Modulator, Continued)

Digital Voice Data

The Command Encoder will accept digital voice data over a twisted pair cable with the following characteristics:

AMPLITUDE - Logic "0": 0.0 volts \pm 0.5 volts
Logic "1": 5.0 volts \pm 1.0 volts

RISE TIME - less than lusec.

32 KHZ Clock

The Command Encoder outputs a gated clock with the following characteristics:

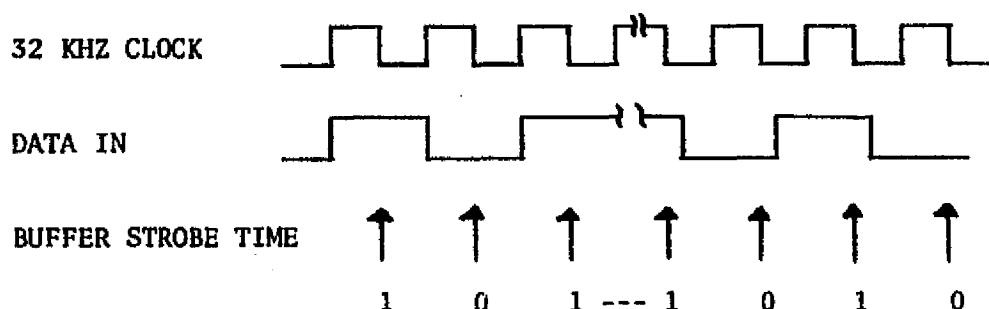


FIGURE 2-15

FREQUENCY - 32.264 KHz \pm 0.005%

AMPLITUDE - Logic "0": 0.0 volts \pm 0.5 volts
Logic "1": 5.0 volts \pm 1.0 volts

DUTY CYCLE (when enabled) - 50 percent \pm 10 percent jitter

RISE TIME - Less than 150 nanosec.

2.8.6 Payload Link Output

The payload link output shall be a modulated baseband to be used as the modulation for the orbiter to payload radio transmitter. Its characteristics are as follows:

Amplitude: \pm 1.0 volts \pm 0.1 volts (R1 = 75)

Rise Time: $< 1\mu$ s (for rectangular signals)

Frequency Range: 100 to 95,000 Hz

B. CE HARDWARE

1.0 COMMAND ENCODER MODULATOR, DIGITAL PORTION

The Modulator is designed to appropriately modulate a sub-carrier with the encoded data in accordance with the selected payload's input requirements.

1.1 Functional Block Diagrams

A functional block diagram of the Modulator is shown in Figure 1-1 and it identifies the major component areas. The P/S (parallel to serial) Converter is used in NASA modes 1, 2 and 6. It converts 16-bit parallel words loaded from the Data Buffer to serial data. The Data Buffer acts as a double buffer for the P/S Converter, thereby increasing the interrupt service window from 1 to 16 bit times (to approximately 396 μ sec.)

The Sub-Carrier Synthesizer is responsible for the generation of the sub-carrier tone frequency. It is generated in a totally digital manner and is capable of generating tones in the range from 1 Hz to 95 KHz. The F_s Buffer acts as a double buffer for the Sub-Carrier Synthesizer. Its presence is dictated by the fact that in NASA 5 and DOD modes, sub-carrier frequency data must occur at the beginning of the bit interval. The Modulation Synthesizer operates in a similar manner to produce the modulation signal and also generates the bit timing signals. The F_M Buffer is the register which contains the value of the modulation frequency to be generated. Double buffering is not required since no change in the modulation frequency takes place during data transmission. The bit timing signals are developed by the M and N Counters. The M Counter determines the length of the tone burst of the sub-carrier synthesizer while the N Counter determines the bit length. The Counter Buffer double buffers data for the M and N Counters. Due to the use of low-power logic and its associated timing problems, a four phase clock is derived from the 2^{22} Hz oscillator. The contents of the Control Register define the mode of operation in which the modulator is to run. The Vector Generator, Bus Timing and Control Logic and 3:8 Decoder form a part of the RP-16 Microprocessor (μ P) interface. The Bus Hung Detector, Power Up Detector and Interval Timer are physically located on one of the modulator logic cards but are not necessary for modulator operation. Their functions will be described in more detail in a later section.

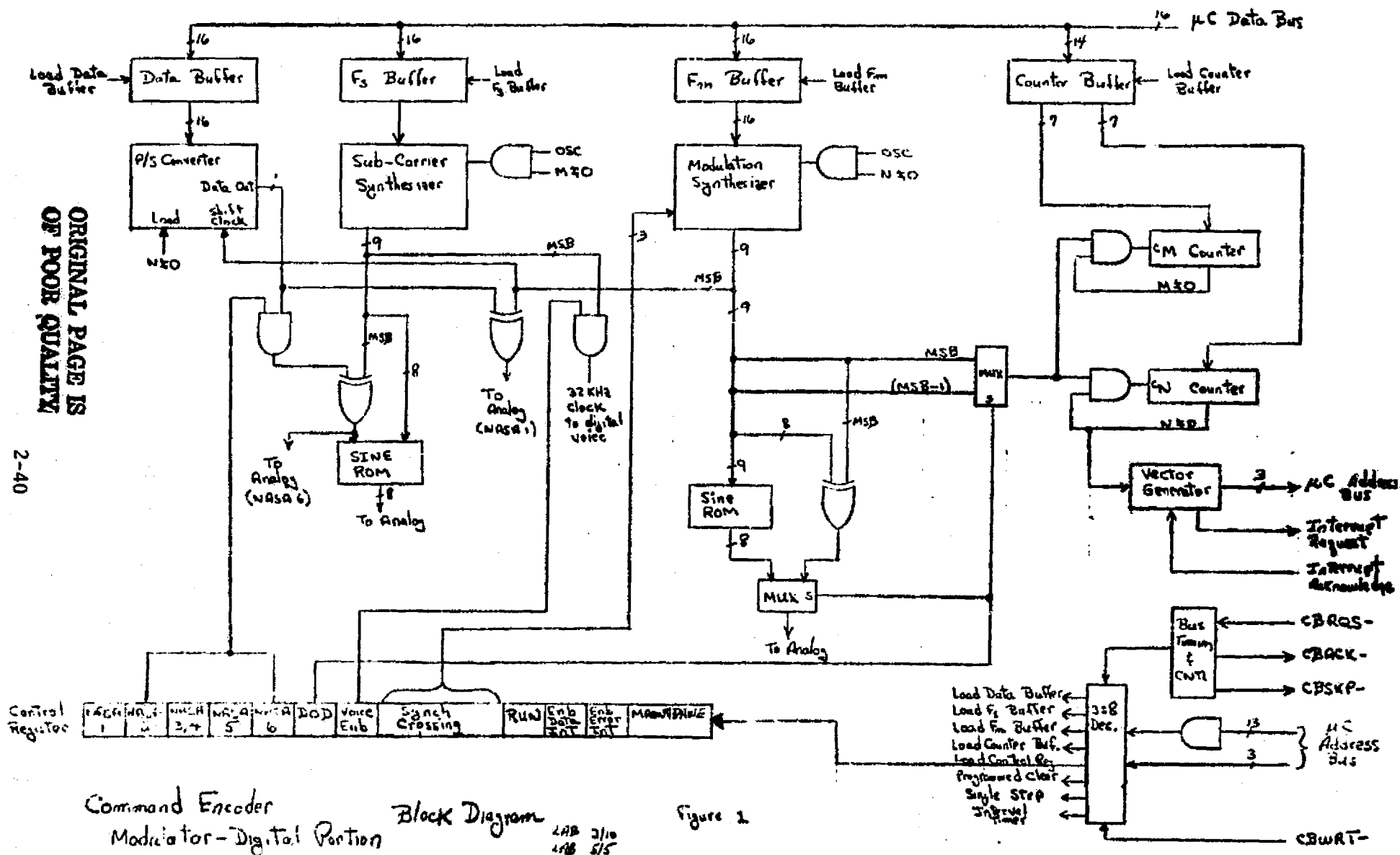
1.2 Modulator Output Specifications

The Command Encoder Digital Modulator possesses the following performance specifications:

Sub-Carrier Synthesizer
Range 1 Hz to 95 KHz
Accuracy $\pm 0.005\%$
Resolution 1 Hz
Total Harmonic Distortion $\leq 5\%$

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2-40



1.2 (Modulator Output Specifications, Continued)

Modulation Synthesizer

Range 1 Hz to 65,535 Hz

Accuracy $\pm 0.005\%$

Resolution 1 Hz

Phase Shift 0 to 7/8 cycle in DOD mode, 0 to 15/16 in NASA modes

Phase Resolution 1/8 cycle in DOD mode, 1/16 cycle in NASA modes

Waveforms Sine or Triangle

Modulation Feedthrough

at least 26 db below sub-carrier

Modulation Shift Time

less than 1 sec.

1.3 Detailed Block Diagrams and Register Formats

Reference should be made to Figures 1-2 & 1-6 for the discussion. Figure 1-2 is a block diagram of the digital portion of the modulator in slightly more detail than Figure 1-1. Figure 1-6 defines the data formats followed by the μP when communicating with the modulator.

1.3.1 Data Buffer

The Data Buffer is a sixteen (16) bit register loadable from the μP which serves as a double buffer for the Parallel to Serial Converter. The most significant bit (MSB) is defined as bit 15 while the least significant bit (LSB) has been assigned to bit 0.

1.3.2 Parallel to Serial Converter

The P/S Converter is loaded sixteen bits at a time from the Data Buffer as a function of the value of the N Counter going to zero. It shifts the data one bit at a time to form a serial stream. When transmitting serial data, the MSB (bit 15) is sent first. The P/S Converter is used in modes, NASA 1, NASA 2 and NASA 6.

1.3.3 Sub-Carrier Synthesizer

F_s Buffer

The F_s Buffer is a sixteen Bit register, the contents of which specify the frequency of the sub-carrier synthesizer. In all modulation modes with the exception of DOD, the MSB is stored in bit 15 with the LSB in bit 0. In DOD mode, the MSB is stored in bit 0, the LSB in bit 1, the (LSB + 1) in bit 2 and so forth until finally the (MSB - 1) is stored in bit 15. The F_s Buffer serves as a double buffer for the F_s Register and as such is loadable by the μP .

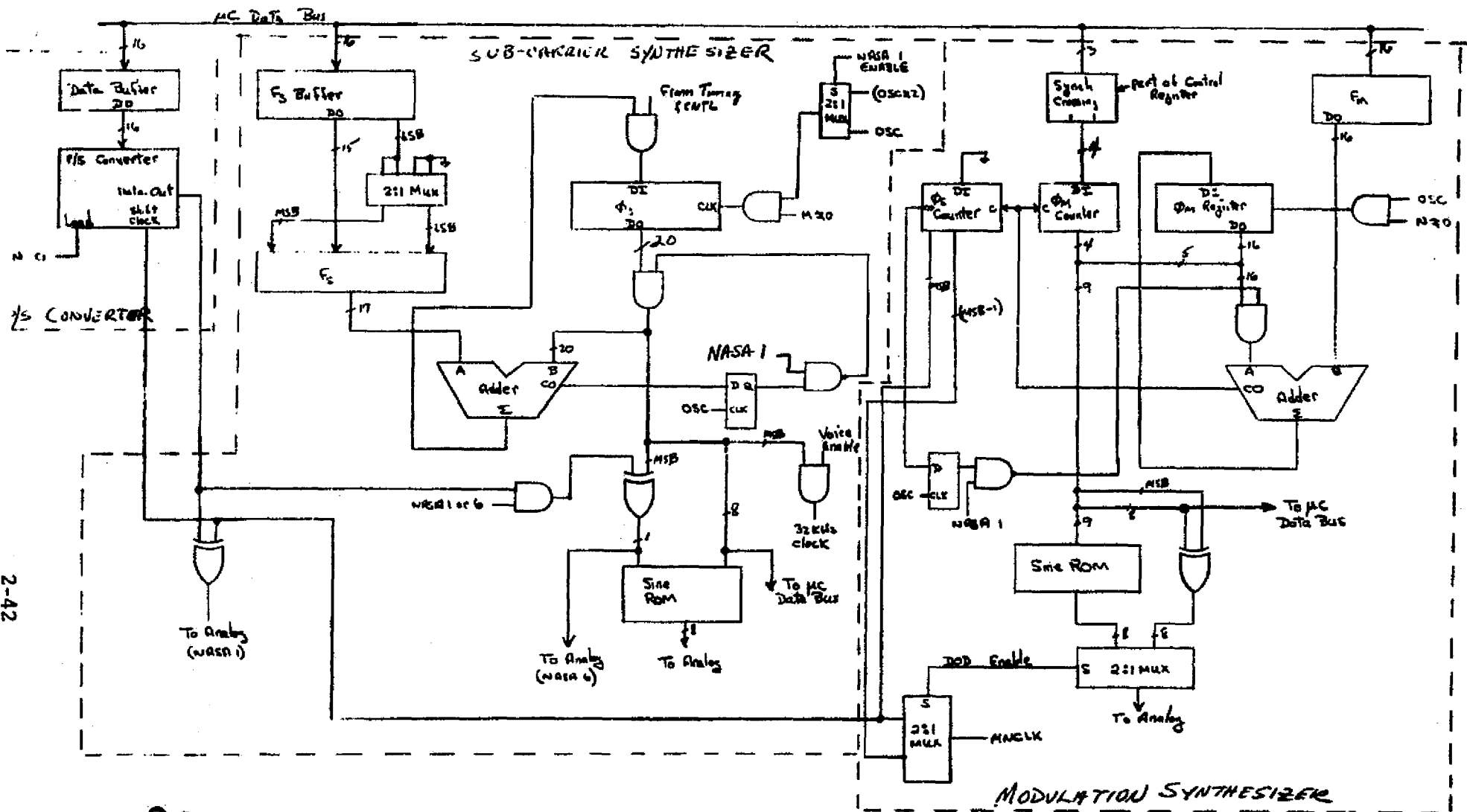
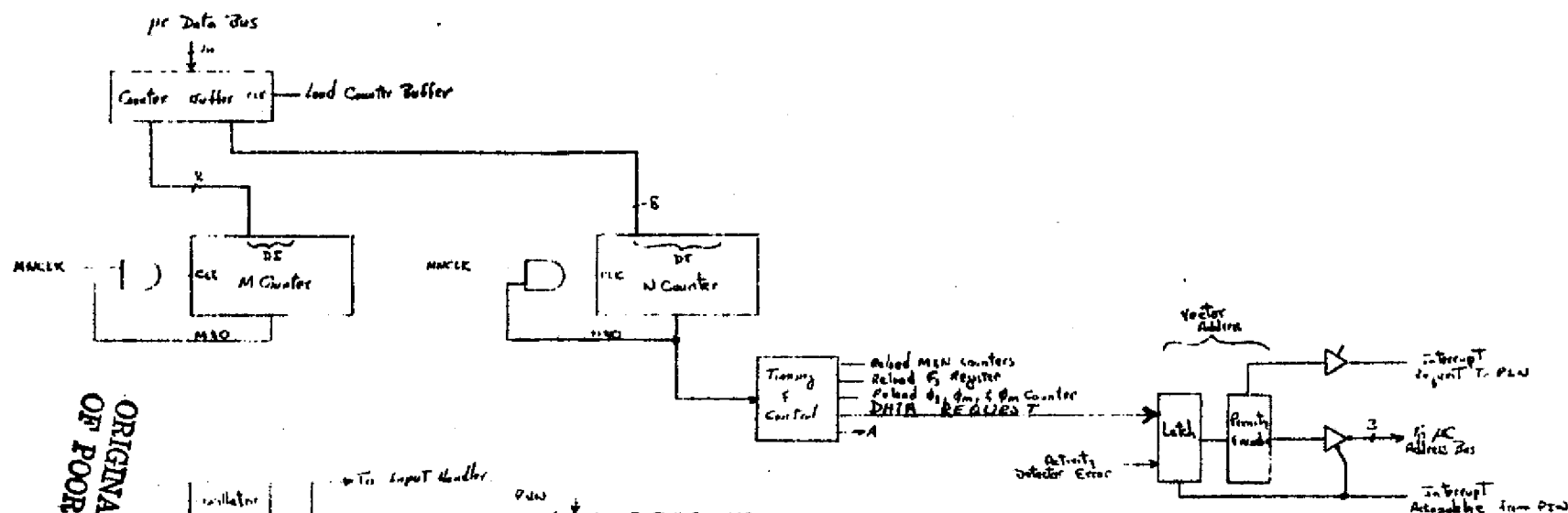


FIGURE 1-2, Sheet 1 of 2

QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
SPECIFIED INCHES			PARTS LIST
CONTR NO.			RAYTHEON COMPAI LEXINGTON, MASS. 02173
DR L.A. Brown		7/21/75	DRAWING TITLE
CHK			Modulator
APPD			Detailed Block Diagram
APPROVED		SIZE	CODE IDENT NO. DRAWING NO.
BY DIRECTION OF		C	455556 Figure 1-2



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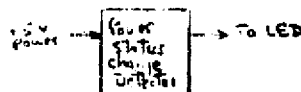
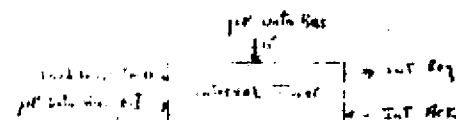
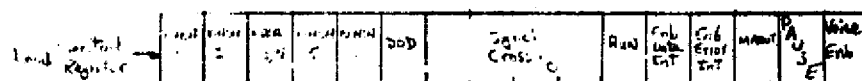
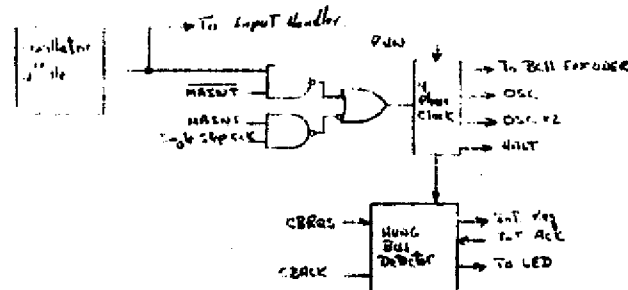
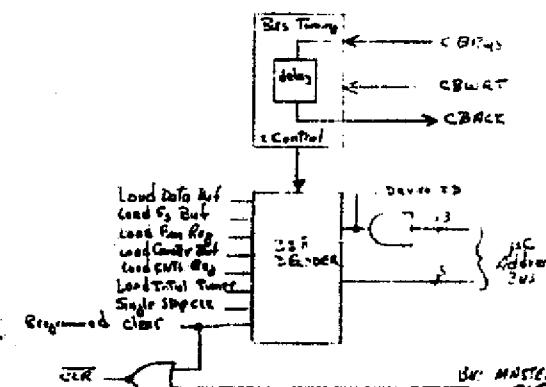


Figure 1-2, Sheet 2 of 2



CITY REQD		CODE IDENT NO	PART NO OR IDENTIFICATION NO	DRAWING OR SPECIFICATION NO	REVISIONS LISTED IN DRAWING	DATE
			PART 215			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES 2 FRACTIONS 2 3 PLACE DECIMALS 2 2 PLACE DECIMALS 2 1 PLACE DECIMALS 2			(ENTER NO) For 1 & 2 Brgs 7/21/76 ENG A B C D			
MATERIAL			APPROVED BY INJECTION OF			
NEXT ASSY			SIZE CODE IDENT NO DRAWING NO 49956 Figure 1-2			
APPLICATION			SCALE SHEET 2 of 2			

1.3.3 (Sub-Carrier Synthesizer, Continued)

F_S Buffer in NASA 1 Mode with Voice

In NASA 1, the sub-carrier synthesizer is used to generate the clock for the voice interface. In order for the clock to be exactly 4/5 of the 40.330 KHz necessary for proper voice data synchronization, it was necessary to increase the sub-carrier synthesizer clock by a factor of 2 to 2²¹ Hz. Therefore, when in the NASA 1 mode with voice, the frequency specified by the F_S buffer should be one-half the desired frequency value.

F_S Register

The F_S Register should not be confused with the F_S Buffer. The F_S Register is a seventeen (17) bit register loaded in parallel from the F_S Buffer. It is possible to load this 17 bit register from a 16 bit buffer once one observes that all DOD frequencies are even (LSB = 0) and all NASA frequencies are lower than 65 KHz (MSB = 0). Hence, in DOD mode, bit 0 of the F_S Register is set to 0 while bit 0 of the F_S Buffer becomes the seventeenth bit of the F_S Register.

Ø_S Register

The Ø_S Register is a twenty (20) bit register which forms a part of the sub-carrier modulator. The register is loaded in parallel with the twenty outputs of the sub-carrier synthesizer adder. The most significant nine (9) bits of this register form the address for the sub-carrier SINE PROM.

Sub-Carrier Adder

The Sub-Carrier Adder is a 20 bit, full binary adder. The contents of the F_S Register are added to the contents of the Ø_S Register and the resultant SUM is returned to the Ø_S Register.

Sub-Carrier Sine PROM

The Sub-Carrier Sine PROM is organized 512 words by 8 bits. The contents of this PROM represent 512 amplitude samples of a SINE wave traveling through 360°. To implement a 512 word by 8-bit memory, four 256 x 4 PROM chips are required.

1.3.3 (Sub-Carrier Synthesizer, Continued)

Figure 1-3 depicts the configuration:

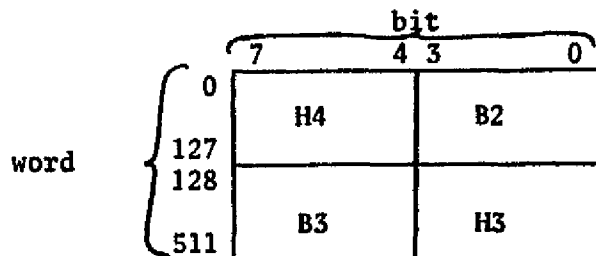


FIGURE 1-3

The contents of each of these four PROM's is given in Tables 1, 2, 3 and 4. The notation used in Tables 1 through 4 is hexadecimal.

1.3.4 Modulation Synthesizer

F_M Register

The F_M Register is a sixteen bit register loadable by the μ P. The MSB is defined as being bit 15 and the LSB has been assigned to bit 0. The contents of this register specify the frequency of the modulation waveform.

TABLE 1

Address	Data
000	0' 0' 0' 0' 0' 0' 0' 0'
008	0' 0' 1' 1' 1' 1' 1' 1'
010	1' 1' 1' 1' 1' 2' 2' 2'
018	2' 2' 2' 2' 2' 2' 2' 2'
020	3' 3' 3' 3' 3' 3' 3' 3'
028	3' 3' 3' 4' 4' 4' 4' 4'
030	4' 4' 4' 4' 4' 4' 4' 4'
038	5' 5' 5' 5' 5' 5' 5' 5'
040	5' 5' 5' 5' 5' 5' 6' 6'
048	6' 6' 6' 6' 6' 6' 6' 6'
050	6' 6' 6' 6' 6' 6' 6' 6'
058	7' 7' 7' 7' 7' 7' 7' 7'
060	7' 7' 7' 7' 7' 7' 7' 7'
068	7' 7' 7' 7' 7' 7' 7' 7'
070	7' 7' 7' 7' 7' 7' 7' 7'
078	7' 7' 7' 7' 7' 7' 7' 7'
080	7' 7' 7' 7' 7' 7' 7' 7'
088	7' 7' 7' 7' 7' 7' 7' 7'
090	7' 7' 7' 7' 7' 7' 7' 7'
098	7' 7' 7' 7' 7' 7' 7' 7'

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(Table 1, Continued)

<u>Address</u>	<u>Data</u>							
0A0	7'	7'	7'	7'	7'	7'	7'	7'
0A8	7'	6'	6'	6'	6'	6'	6'	6'
0B0	6'	6'	6'	6'	6'	6'	6'	6'
0B8	6'	6'	6'	5'	5'	5'	5'	5'
0C0	5'	5'	5'	5'	5'	5'	5'	5'
0C8	5'	4'	4'	4'	4'	4'	4'	4'
0D0	4'	4'	4'	4'	4'	4'	3'	3'
0D8	3'	3'	3'	3'	3'	3'	3'	3'
0E0	3'	2'	2'	2'	2'	2'	2'	2'
0E8	2'	2'	2'	2'	1'	1'	1'	1'
0F0	1'	1'	1'	1'	1'	1'	1'	0'
0F8	0'	0'	0'	0'	0'	0'	0'	0'
FIN								

CE-08 Location G4

CE-06 Location H4

TABLE 2

<u>Address</u>	<u>Data</u>							
000	0'	2'	3'	5'	6'	8'	9'	B'
008	C'	E'	0'	1'	3'	4'	6'	7'
010	9'	A'	C'	D'	F'	0'	2'	3'
018	5'	6'	8'	9'	B'	C'	E'	F'
020	1'	2'	3'	5'	6'	8'	9'	A'
028	C'	D'	F'	0'	1'	3'	4'	5'
030	7'	8'	9'	A'	C'	D'	E'	F'
038	1'	2'	3'	4'	5'	6'	8'	9'
040	A'	B'	C'	D'	E'	F'	0'	1'
048	2'	3'	4'	5'	6'	7'	8'	9'
050	A'	A'	B'	C'	D'	E'	F'	F'
058	0'	1'	1'	2'	3'	3'	4'	5'
060	5'	6'	6'	7'	8'	8'	9'	9'
068	A'	A'	A'	B'	B'	C'	C'	C'
070	D'	D'	D'	D'	E'	E'	E'	E'
078	E'	F'	F'	F'	F'	F'	F'	F'
080	F'	F'	F'	F'	F'	F'	F'	F'
088	E'	E'	E'	E'	E'	D'	D'	D'
090	D'	C'	C'	C'	B'	B'	A'	A'
098	A'	9'	9'	8'	8'	7'	6'	6'
0A0	5'	5'	4'	3'	3'	2'	1'	1'
0A8	0'	F'	F'	E'	D'	C'	B'	A'
0B0	A'	9'	8'	7'	6'	5'	4'	3'
0B8	2'	1'	0'	F'	E'	D'	C'	B'
0C0	A'	9'	8'	6'	5'	4'	3'	2'
0C8	1'	F'	E'	D'	C'	A'	9'	8'
0D0	7'	S'	4'	3'	1'	0'	F'	D'
0D8	C'	A'	9'	8'	6'	5'	3'	2'

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(Table 2, Continued)

Address	Data
0E0	1' F' E' C' B' 9' 8' 6'
0E8	5' 3' 2' 0' F' D' C' A'
0F0	9' 7' 6' 4' 3' 1' 0' E'
0F8	C' B' 9' 8' 6' 5' 3' 1'
FIN	

CE-08 Location A6

CE-06 Location B2

TABLE 3

Address	Data
300	F' F' F' F' F' F' F' F'
308	F' F' F' E' E' E' E' E'
310	E' E' E' E' E' E' D' D'
316	D' D' D' D' D' D' D' D'
320	C' C' C' C' C' C' C' C'
328	C' C' C' C' B' B' B' B'
330	B' B' B' B' B' B' B' B'
338	A' A' A' A' A' A' A' A'
340	A' A' A' A' A' A' A' A'
346	9' 9' 9' 9' 9' 9' 9' 9'
350	9' 9' 9' 9' 9' 9' 9' 9'
358	9' 8' 8' 8' 8' 8' 8' 8'
360	8' 8' 8' 8' 8' 8' 8' 8'
368	8' 8' 8' 8' 8' 8' 8' 8'
370	8' 8' 8' 8' 8' 8' 8' 8'
378	8' 8' 8' 8' 8' 8' 8' 8'
380	8' 8' 8' 8' 8' 8' 8' 8'
388	8' 8' 8' 8' 8' 8' 8' 8'
390	8' 8' 8' 8' 8' 8' 8' 8'
398	8' 8' 8' 8' 8' 8' 8' 8'
3A0	8' 8' 8' 8' 8' 8' 8' 8'
3A8	9' 9' 9' 9' 9' 9' 9' 9'
3B0	9' 9' 9' 9' 9' 9' 9' 9'
3B8	9' 9' A' A' A' A' A' A'
3C0	A' A' A' A' A' A' A' A'
3C8	A' B' B' B' B' B' B' B'
3D0	E' B' B' B' B' B' C' C' C'
3D8	C' C' C' C' C' C' C' C'
3E0	C' D' D' D' D' D' D' D'
3E8	D' D' D' E' E' E' E' E'
3F0	E' E' E' E' E' E' F' F'
3F8	F' F' F' F' F' F' F' F'
FIN	

CE-08 Location A5

CE-06 Location B3

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TABLE 4

Address	Data
020	F' E' D' B' A' 8' 7' 5'
028	4' 2' 0' F' D' C' A' 9'
010	7' 6' 4' 3' 1' 0' E' D'
018	B' A' 8' 7' 5' 4' 2' 1'
020	F' E' D' B' A' 8' 7' 6'
028	4' 3' 1' 0' F' D' C' B'
030	9' 8' 7' 6' 4' 3' 2' 1'
038	F' E' D' C' B' A' 8' 7'
040	6' 5' 4' 3' 2' 1' 0' F'
048	E' D' C' B' A' 9' 8' 7'
050	6' 6' 5' 4' 3' 2' 1' 1'
058	0' F' F' E' D' D' C' B'
060	B' A' A' 9' 8' 8' 7' 7'
060	6' 6' 6' 5' 5' 4' 4' 4'
070	3' 3' 3' 3' 2' 2' 2' 2'
078	2' 1' 1' 1' 1' 1' 1' 1'
080	1' 1' 1' 1' 1' 1' 1' 1'
088	2' 2' 2' 2' 2' 3' 3' 3'
090	3' 4' 4' 4' 5' 5' 6' 6'
096	6' 7' 7' 8' 8' 9' A' A'
0A0	B' B' C' D' D' E' F' F'
0A8	2' 1' 1' 2' 3' 4' 5' 6'
0B0	6' 7' 8' 9' A' B' C' D'
0B8	E' 5' 3' 1' 2' 3' 4' 5'
0C0	6' 7' 5' A' B' C' D' E'
0C8	F' 1' 2' 3' 4' 6' 7' 8'
0D0	9' E' C' D' F' 0' 1' 3'
0D8	4' 6' 7' 8' A' B' D' E'
0E0	F' 1' 2' 4' 5' 7' 8' A'
0E6	B' D' E' 0' 1' 3' 4' 6'
0F2	7' 9' A' C' D' F' 0' 2'
0F8	4' 5' 7' 8' A' B' D' F'
FIN	

CE-08 Location G5

CE-06 Location H3

1.3.4 (Modulation Synthesizer, Continued)

 Φ_M Register

The Φ_M Register is a sixteen bit register which forms a part of the modulation synthesizer. This register is loaded in parallel with data from the sixteen outputs of the modulation synthesizer adder. The most significant five (5) bits of the Φ_M Register form a part of the modulation synthesizer Sine PROM.

1.3.4 (Modulation Synthesizer, Continued)

ϕ_M Counter

The ϕ_M Counter is a four (4) bit binary counter whose outputs form the most significant four bits of address of the modulation synthesizer Sine PROM. This counter also handles the phase shift requirement of the modulation waveform. The counter is incremented by the carry overflow from the modulation synthesizer adder.

ϕ_S Counter

The ϕ_S Counter is a four bit binary counter whose task is to define the length of the bit interval. This counter is also incremented by the carry overflow from the modulation synthesizer adder.

Modulation Synthesizer Adder

The Modulation Synthesizer Adder is a sixteen (16) bit full binary adder. The contents of the F_M Register and the ϕ_M Register are summed and the result is stored in the ϕ_M Register. The "carry out" of the adder is used to increment the ϕ_S Counter and the ϕ_M Counter.

Modulation Sine PROM

The Modulation Sine PROM is organized 512 words by 8 bits. The contents of the PROM represent 512 samples of a Sine wave traveling through 360°. The configuration of the Modulation Synthesizer SINE PROM is similar to that used for the Sub-Carrier. Figure 1-4 shows this configuration:

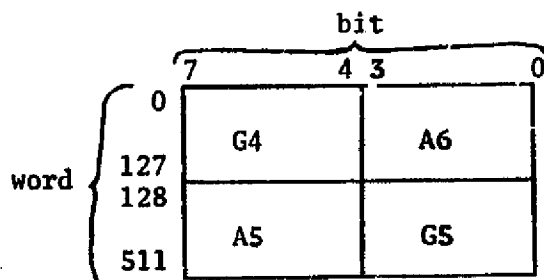


FIGURE 1-4

The hexadecimal values of each of these PROM's is given in Tables 1, 2, 3 and 4.

Modulation Synthesizer 2:1 Multiplexer

In NASA modes 2, 3, 4 and 5, the function of the modulation synthesizer is to generate a Sine wave. In modes DOD 1-13, the modulation synthesizer must generate a triangular waveform. The 2:1 Multiplexer sends either the output of the PROM or the output from the Exclusive-OR triangle generator gates to the analog logic.

1.3.4 (Modulation Synthesizer, Continued)

Modulation Synthesizer Exclusive-OR Gates

These Exclusive-OR gates modify the Modulation Synthesizer Sine PROM address to form the DOD triangular waveform per the following algorithm:

- If address bits 7 and 8 are equal to 0 ($0^\circ - 90^\circ$),
do not modify address bits 0 through 8.
- If address bit 7 is equal to 1 and bit 8 is equal to 0
($90^\circ - 180^\circ$), complement bits 0 through 7. Do
not modify bit 8.
- If address bit 7 is equal to 0 and bit 8 is equal to 1
($180^\circ - 270^\circ$), complement bits 0 through 7.
Do not modify bit 8.
- If address bits 7 and 8 are equal to 1 ($270^\circ - 360^\circ$),
do not modify address bits 0 through 8.

This algorithm when followed will result in a waveform similar to that drawn in Figure 1-5.

Counter Buffer

The Counter Buffer is a sixteen (16) bit register loadable by the μP . It double buffers data for the M and N Counters. Bits 0 through 7 have been assigned for the storage of M Counter data with bit 0 the LSB and bit 7 the MSB. Bit 8 has been assigned the LSB of the N Counter data with bit 15 the MSB.

M Counter

The M Counter is an eight (8) bit binary counter which is loaded from bits 0 through 7 of the Counter Buffer. Its purpose is to regulate the amount of time the sub-carrier synthesizer is allowed to operate. If the value of the M Counter is not equal to zero, then the sub-carrier synthesizer is free to run. This counter is incremented at the end of every bit interval.

N Counter

The N Counter is an eight (8) bit binary counter which is loaded from bits 8 through 15 of the Counter Buffer. The value of the N Counter is the number of bit intervals the modulation synthesizer is allowed to run.

1.3.5 Control Register

The control register is a sixteen (16) bit register loadable by the μP . The contents of this register defines what action the modulator is to perform. Reference should be made to Figure 1-6 for this discussion.

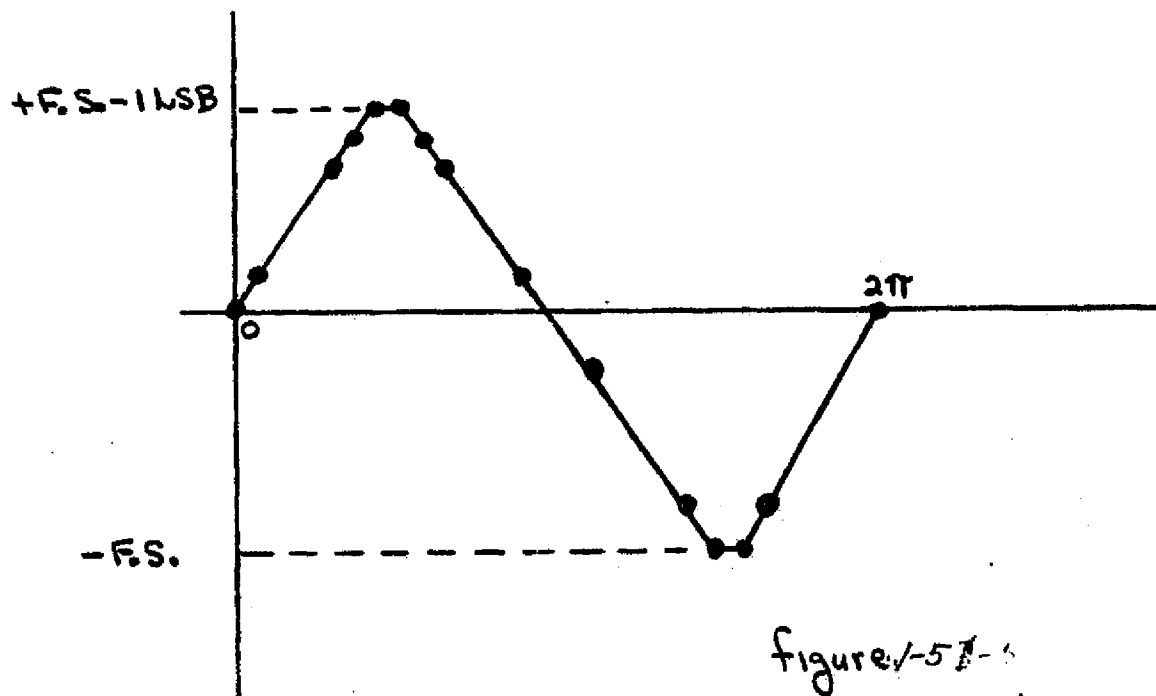


figure 5-1-6
Plot of Triangular Waveform
Algorithm

Octal Address	Function	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
176100	Load Control Register	NASA 1	NASA 2	NASA 3,4	NASA 5	NASA 6	DOD	SYNC MSB		SYNC	SYNC	RUN	ENB DATA Int.	ENB Error Int.	MAINT	PAUSE	Voice Enable
176101	Load F _s Buffer	MSB ← → LSB															
176102	Load F _m Register	MSB ← → LSB															
176103	Load Counter Buffer	MSB ← N Counter → LSB								MSB ← M Counter → LSB							
176104	Load Data Buffer	MSB ← → LSB															
176105	Load & start/stop Interval Timer	Load/clear	MSB ← → LSB														
176106	Programmable Single Step Clock																
176107	Programmable Modulator Clear																
176100-176107	Read PROM Address Register	MSB-1 ← Modulation PROM Address → LSB								MSB-1 ← Sub-Carrier PROM Address → LSB							

Figure 1-6
Modulator Register Addresses
&
Data Formats

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1.3.5 (Control Register, Continued)

bits 15, 14, 13, 12, 11 and 10 define what modulation mode is to be followed. Only one mode may be selected at any one time.

bits 9, 8, 7 and 6 control the phase shift of the modulation synthesizer waveform. The amount of phase shift may be determined per Figures 1-7 and 1-8.

CONTROL REGISTER BIT				AMOUNT OF PHASE SHIFT REQUIRED
Bit 9	Bit 8	Bit 7	Bit 6	
0	0	0	0	1/2 cycle
0	0	0	1	7/16 cycle
0	0	1	0	3/8 cycle
0	0	1	1	5/16 cycle
0	1	0	0	1/4 cycle
0	1	0	1	3/16 cycle
0	1	1	0	1/8 cycle
0	1	1	1	1/16 cycle
1	0	0	0	0 cycle

FIGURE 1-7
Phase Shift of the Modulation Synthesizer
in NASA Mode 5

CONTROL REGISTER BIT				AMOUNT OF PHASE SHIFT REQUIRED
Bit 9	Bit 8	Bit 7	Bit 6	
0	0	0	0	1 cycle
0	0	0	1	$1/2 + 1/4 + 1/8 = 7/8$ cycle
0	0	1	0	$1/2 + 1/4 = 3/4$ cycle
0	0	1	1	$1/2 + 1/8 = 5/8$ cycle
0	1	0	0	1/2 cycle
0	1	0	1	$1/8 + 1/4 = 3/8$ cycle
0	1	1	0	1/4 cycle
0	1	1	1	1/8 cycle
1	0	0	0	0

FIGURE 1-8
Phase Shift of the Modulation Synthesizer
in DOD Modes 1 through 13

1.3.5 (Control Register, Continued)

bits 8, 7, and 6 control the phase shift of the modulation synthesizer waveform. The amount of phase shift may be determined per Figure 1-5.

bit 5 is the "RUN" bit. If set, the four-phase clock to the synthesizers is enabled. If it is desired to stop the modulator, this bit should be reset (set to "0"). The modulator will complete the processing of any partially completed data and then stop.

bit 4 if set (equal to a logic 1) will enable modulator data service interrupt requests. If this bit is reset, all modulator data service interrupts to the Command Encoder μ P will be inhibited.

bit 3 if set will enable the modulator error interrupt to be sent to the μ P. If reset, the error interrupt will be inhibited. Receipt of this interrupt is an indication that the "activity detector" monitoring the analog output of the modulator has sensed an error.

bit 2 is the maintenance or test bit. If set, the 2²² Hz oscillator is multiplexed off and a programmable single step clock is enabled. The bit should only be set when maintenance testing is desired.

bit 1 is the PAUSE bit. This bit normally is only used in the NASA 5 mode. If set, the digital portion of the modulator continues to run, but the cross-link output is forced to zero volts. The use of this bit permits the modulator to continue to generate data interrupts to the μ P to maintain bit intervals. The modulator will enter or exit the PAUSE mode only at the start of a bit interval.

bit 0 if set (equal to logic "1") enables the 32 KHz clock used in the Voice Interface. This bit should be set only if NASA 1 mode with voice has been selected.

1.4 Microprocessor Interface

The modulator interface to the Command Encoder RP-16 Microprocessor (μ P) is composed of the following parts:

1.4.1 Bus Timing and Control

The Bus Timing and Control Logic is composed of the necessary circuitry to interface with the μ P Bus Control signals; CBRQS-, CBACK-, and CBWRT-. CBRQS- is the μ P bus "request" signal; CBACK- is generated by the modulator and is the μ P bus "acknowledge" signal; and CBWRT- is the μ P bus "write" signal indicating whether the current request cycle is a "read" or "write".

1.4.1 (Bus Timing and Control, Continued)

3:8 Decoder

The 3:8 Decoder combined with the Bus Timing and Control Logic decodes the μ P address bus to determine which function code is being selected. Figure 1-6 lists the octal addresses of each function decode. Note that all the function codes with the sole exception of the READ PROM ADDRESS REGISTER is a μ P "write" operation. The modulator will respond to a bus request to "read" if any of the addresses assigned to the modulator are active. In each case, this "read" will gate onto the μ P data bus the eight least significant bits of both the Sub-Carrier and Modulation Synthesizer PROM address registers. This latter feature is most often used in the Maintenance mode. Three of the "write" function decodes deserve special attention. Reference the following sections.

Function Decode

Load and START/STOP Interval Timer.

If the μ P performs a "write" request to octal address 176105 and if μ P Data Bus Bit 15 is a "1", then a 16-bit binary counter is loaded from the μ P bus with the contents specified by μ P Data Bus Bits 0 through 14. The counter LSB is preset to 0 by logic. Reference Figure 1-6. This also enables a 220 Hz clock to begin clocking a binary counter. The counter continues to decrement until the underflow condition exists whereupon an interrupt to the μ P will be generated. If at any time during the counting process if the μ P performs a "write" request to octal address 176105 and μ P Data Bit 15 is equal to "0", then the counter is cleared, the interval timer interrupt is masked and the counter clock is disabled.

The maximum interval which may be set is 62.5 msec.

Programmable Single Step Clock

In the maintenance mode, the 222 Hz oscillator is disabled. Each time this function code is executed, it represents one cycle of the 222 Hz clock.

Programmable Modulator Clear

This function code, when executed, will initialize the Modulator in a similar manner as the Master Clear (MSTCL-) signal on the μ P bus with the exception that the four-phase clock circuitry is not re-initialized.

1.4.2 Interrupt Logic

The modulator has three separate interrupt lines going to the Priority Interrupt Network (PIN). Reference the following sections. Note: the order of the subsequent sub-paragraphs is not intended to dictate the level of interrupts as seen by the PIN.

1.4.2 (Interrupt Logic, Continued)

Modulator INterrupt Request Number 1

This interrupt is generated if either the modulator is requesting data or if the "activity detector" on the cross-link output has sensed an error. Separate mask functions (see Figure 1-6) permit the disabling of either or both conditions. When the μP responds with the interrupt acknowledge pulse, the modulator will vector the program to the appropriate service subroutine. The interrupt vector trap addresses are defined in Figure 1-9.

Reason for Interrupt		Least Significant 3 vector address bits		
data service	activity detector error	CBA02	CBA01	CBA00
0	1	0	0	1
1	0	0	0	0
1	1	0	0	1

FIGURE 1-9

Notes:

1. An "activity detector error" takes priority over a data service request.
2. The modulator only supplies the three (3) least significant address bits. The remainder are supplied by the Priority Interrupt Network.

Modulator Interrupt Request Number 2

This interrupt is generated by the interval timer. Since it is a dedicated interrupt, no extra vectoring logic is necessary. The trap address will be assigned by the PIN.

Modulator Interrupt Request Number 3

This interrupt is generated by the Hung Bus Detector. Since it is a dedicated interrupt, no extra vectoring logic is necessary. The trap address will be assigned by the PIN.

1.4.3 Hung Bus Detector

A "Hung Bus" condition exists whenever the μP issues a bus request (CBRQS) and a peripheral (or memory) does not issue a bus acknowledge (CBACK). If the acknowledge is not issued the μP effectively would remain in a loop forever. The Hung Bus Detector will detect the condition and release the μP by issuing a CBACK. In order to inform the μP that such an event has occurred, a LED on the Command Encoder front panel will be lit and an interrupt to the μP will be generated. The detector will allow an unanswered CBRQS for approximately 16 μsec . before taking action. The LED may be extinguished either by issuance of the modulator programmed clear function or by the μP bus Master Clear.

1.4.4 Power Status Change Detector

A circuit to detect that the plus five (+5) volt power supply has been turned ON has been included. If the +5 volt supply is initially OFF and then turned ON, a LED on the Command Encoder front panel will be lit. This LED may be extinguished only by the μP bus Master Clear signal.

1.4.5 Four-Phase Clock

Extensive use of low-power logic has necessitated the use of a four-phase clock. The outputs of the clock generator are shown in Figure 1-10.

1.5 Hardware State Following a Microprocessor Master Clear

If the μP bus signal MSTCL- (Master Clear) is activated, the modulator will assume the following state.

- a. The Control Register will be cleared (all bits set to "0")
- b. The Power Status Change Detector will be reset.
- c. The Interval Timer will be reset and halted.
- d. The Hung Bus Detector will be reset.
- e. The ϕ_S Register will be reset.
- f. The ϕ_M Counter, ϕ_M Register and ϕ_S Counter will be reset.
- g. The Counter Buffer and M and N Counters will be reset.
- h. The Four-Phase Clock will be cleared and re-enabled.

1.6 Software Considerations

The following series of flowcharts (Figures 1-11 through 1-17) are intended to be a rough outline of the modulator software driver requirements.

1.7 Built-In Test Equipment (BITE)

Two special features were added to the modulator design to facilitate the logic checkout and to support on-site maintenance. This first feature is a programmable single step clock. By setting the Maintenance bit in the Control Register, the free running 222 Hz. oscillator is gated off. Every time the programmable single step clock function code is executed, it represents one cycle of the 222 Hz. clock. The second special feature is the ability to interrogate the eight (8) least significant bits of both the sub-carrier and modulation synthesizer PROM address registers. The format of both these codes is shown in Figure 1-6.

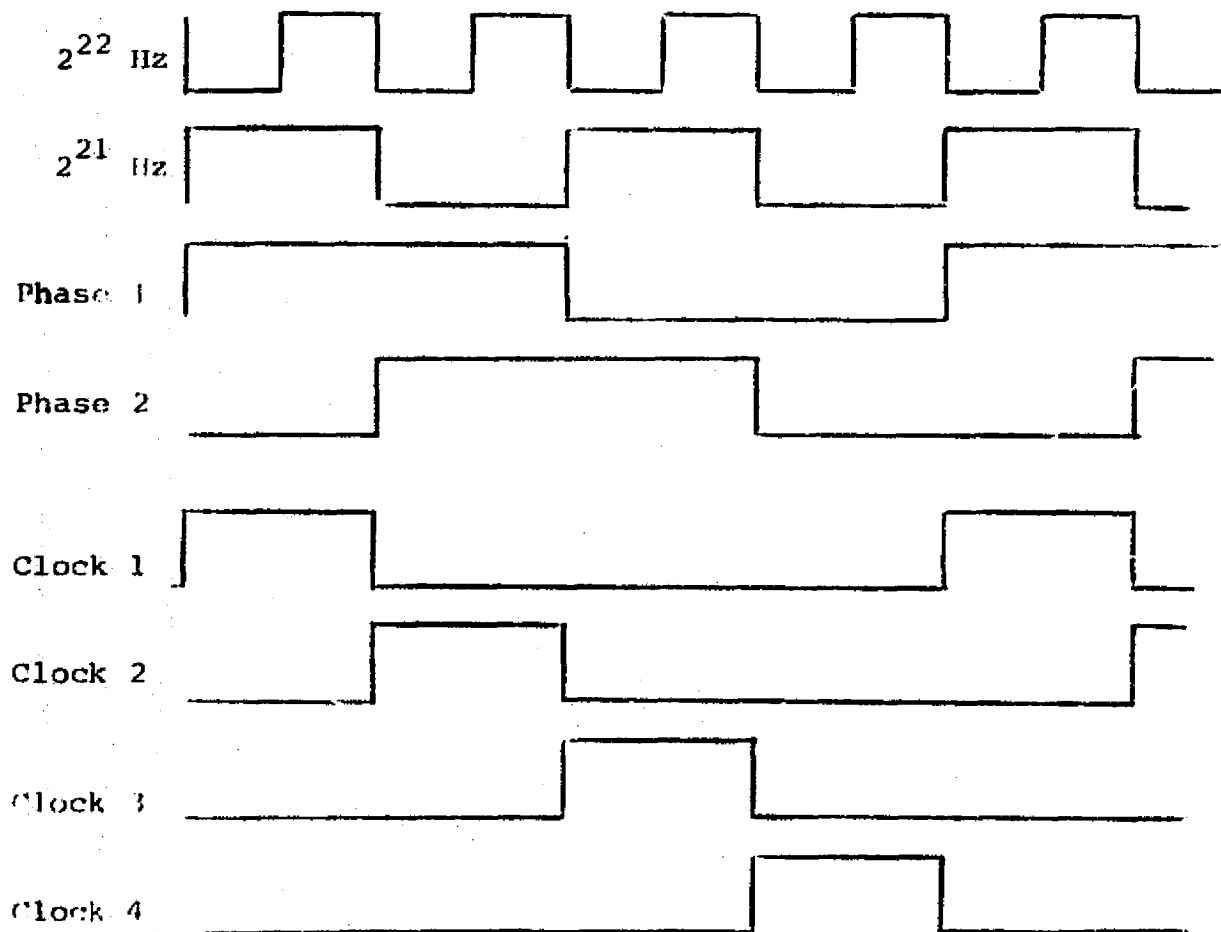
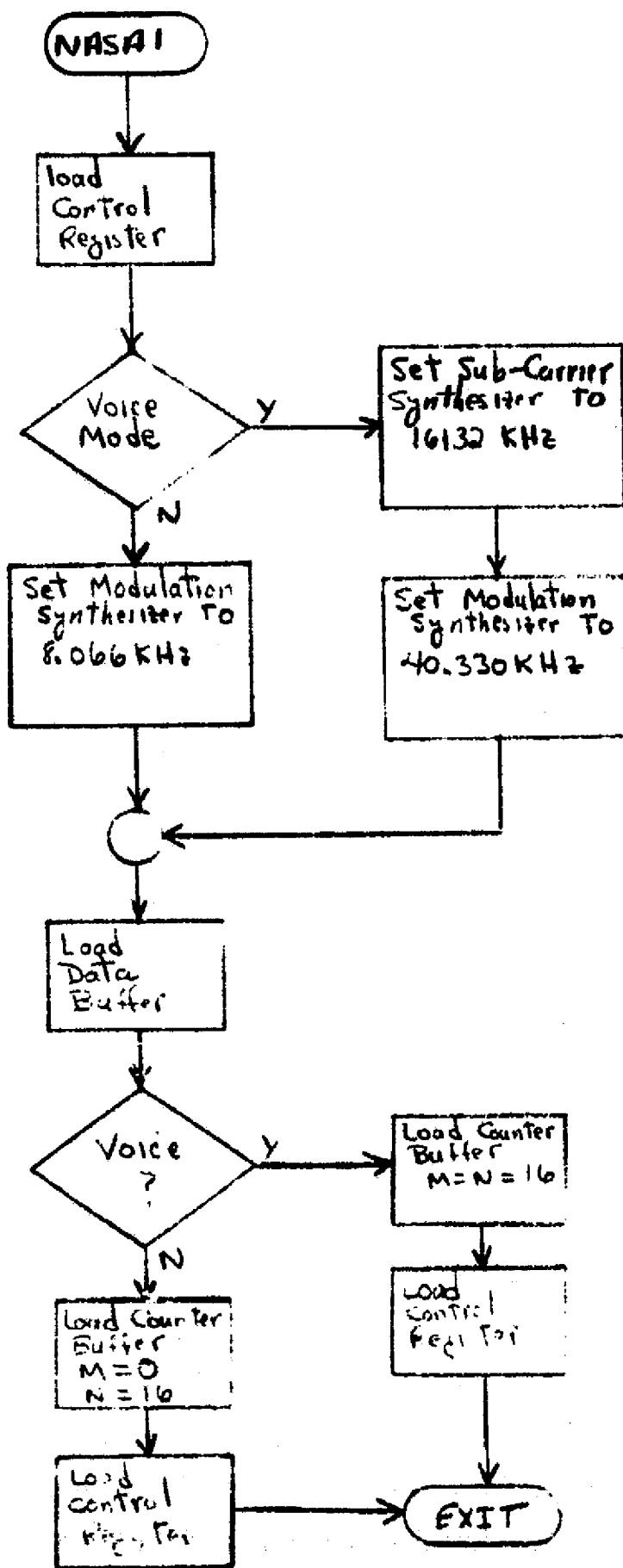


Figure 1-10 /
Four-Phase Clock Timing

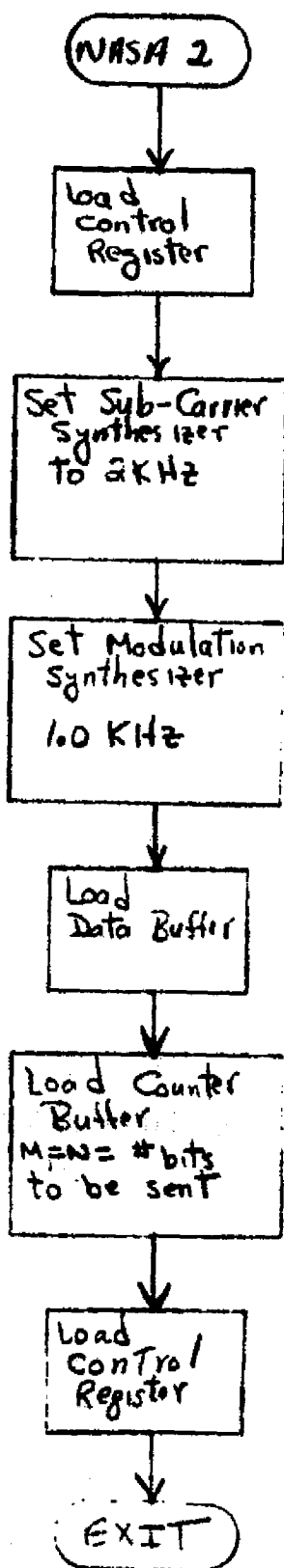


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figure 1-11

N.H.H.

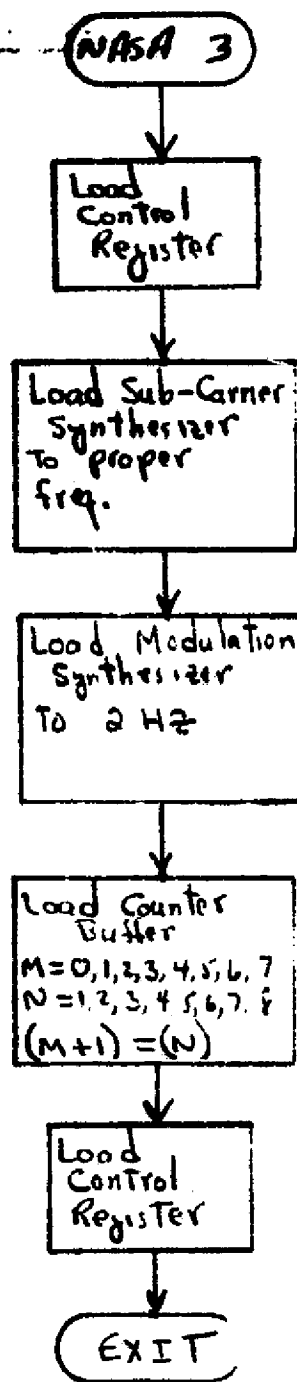
LARE 3/19/75
5/5/75



- 1-12

NASA 2

LKIE 3/19/75
5/1/75



Address Freq

1025 Hz
1097
1174
1262

1352 Hz
1447
1549
1750

1600 Hz
4245
4550
5155

5451 Hz
5790
6177

Execute Freq

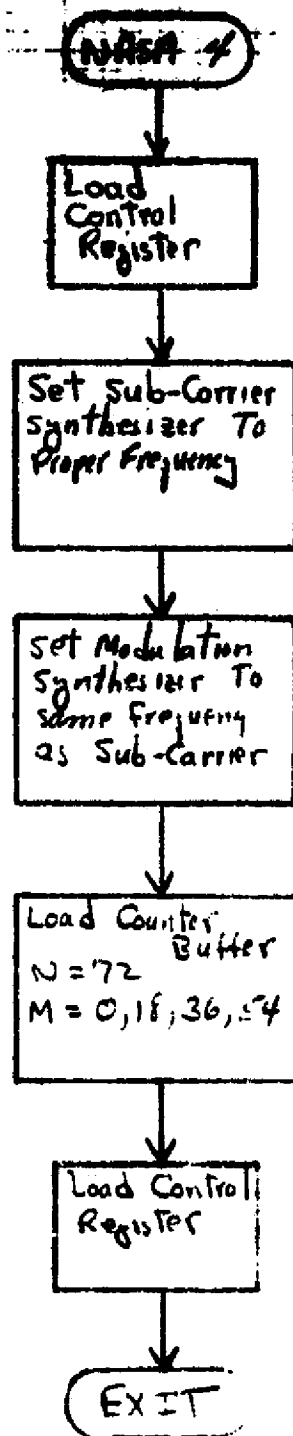
2000 Hz
2270
2650
3000

3305 Hz
3621
3850

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1-13
NASA 3

11B 11/17



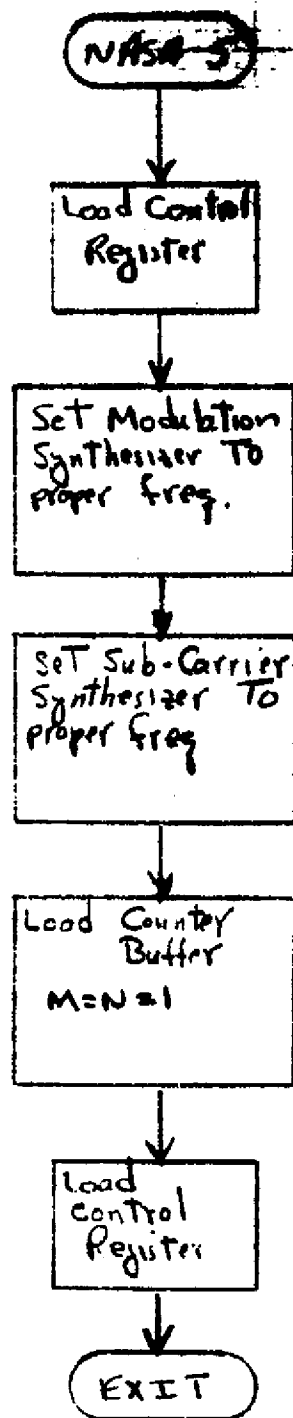
$7000 \text{ Hz} < \text{Freq} < 11024 \text{ Hz}$

$M=0 = \text{blank}$
 $=18 = \text{Logic 0}$
 $=36 = \text{Logic 1}$
 $=54 = \text{Synch code}$

Figure 1-14

NACA 4

LAB $\sim 1/10/2 =$
 $\sim 1/17 =$



proper freq. are 2^i bits/sec $3 \leq i \leq 10$
 or $100j$ bits/sec $1 \leq j \leq 12$

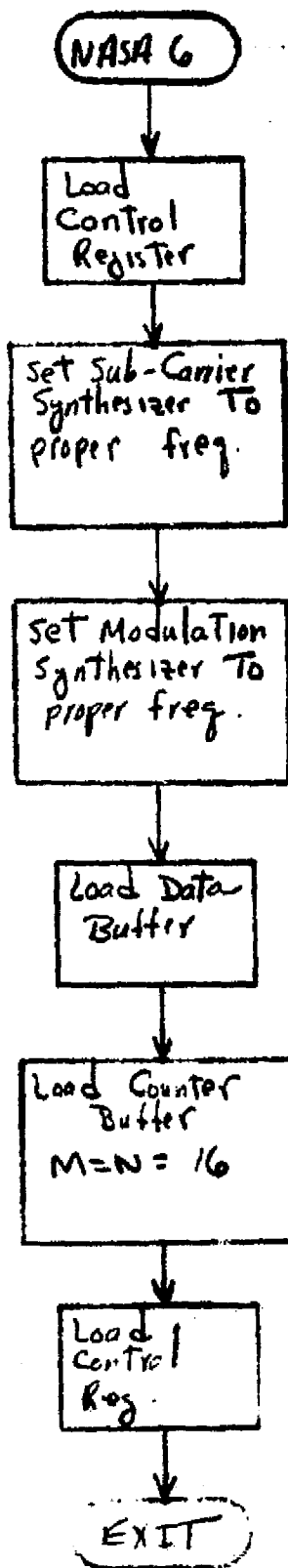
Tone $f_1 = \log_{10} 0$
 Tone $f_2 = \log_{10} 1$ } $7\text{KHz} \leq f_1 \text{ and } f_2 \leq 21\text{KHz}$

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Sheet 1-15

W.A.H.

LA 3/11/77
 1/15

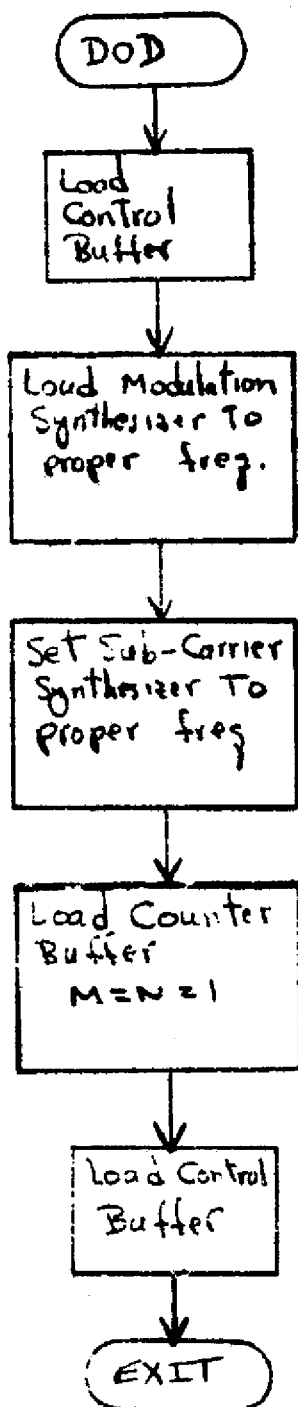


$$2^1 \leq f_{\text{freq}} \leq 2^{12}$$

Figure 1-16

NASA 6

AB 3/19/75
5/5/75



freq = 500 Hz or 1 KHz

space = 65 KHz
 zero = 76 KHz
 one = 95 KHz

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1-17

DOJ 1-13

LAE 1/20/75
 5/1/75

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1.8 Schematics

The digital portion of the modulator is partitioned onto three separate wire wrap cards. The drawing numbers of each card are listed below:

<u>Dwg. No.</u>	<u>Title</u>	<u>Logic</u>
893183	Modulator Synthesizer	Modulation Synthesizer, M Counter, N Counter, Counter Buffer, Four-Phase Clock
893184	Sub-Carrier Synthesizer	Sub-Carrier Synthesizer, Data Buffer, Parallel/Serial Converter
893185	μP Interface	Control Register, Address and Function Decoders, Vector Generator, Power Status Change Detector, Interval Timer, Hung Bus Detector

2.0 MODULATOR ANALOG PORTION

This section describes the design of the analog portion of the Command Encoder. Its function is to provide the subcarrier and modulation waveforms for the various NASA codes under control of the digital portion of the modulator. It also provides the payload crosslink output cable driver and output activity detector for the BITE function.

References:

- (1) Space Shuttle Onboard Command Encoder Design Definition Study
Final Report, FR73-4525, 15 Dec. 1973
- (2) Command Encoder Specification, Sales Order no. 81364 rev. 0,
20 Jan. 1975

2.1 Functional Description

2.1.1 Requirements/Performance

Subcarrier

range 1 to 95 KHz
total harmonic distortion <5%

Modulation

waveform	sine or triangle
range	1 to 65,535 Hz
phase shift	0 to 7/8 cycle
phase resolution	1/8 cycle (45°)

Modulation Feedthrough <-26db

Modulator Shift Time <1 sec.

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2.1.1 (Requirements/Performance, Continued)

Payload Link Output

amplitude	$\pm 1V \pm 10\%$ ($\pm 1db$)
load impedance	75 ohms
rise time (for NASA 1 & 6)	$< 1 \text{ usec}$
jitter (for NASA 1 & 6)	$< 5 \text{ NS}$
frequency range	100 to 95,000 Hz

Activity Detector

signal	TTL compatible
"1"	fault
"0"	output normal

Digital Inputs

impedance	TTL compatible
level	

NASA 2 Carrier

frequency	70 KHz
accuracy	$\pm 1\%$
deviation	$\pm 5 \text{ KHz}$

Oscillator Output

frequency	4,194,304 Hz (2^{22} Hz) actual unit is 4.1943 MHz
accuracy	$\pm .001\%$
temperature	$\pm .001\%$
stability	0°C to 50°C
output	10 TTL loads
"0"	$< .4V$ @ $-1A \text{ ma}$
"1"	$> 2.4V$ @ -2 ma

Power Requirements

+ 5 VDC @ 100 ma
-15 VDC @ 200 ma
+15 VDC @ 200 ma

2.1.2 Assumptions/Tradeoffs

The conceptual design and design tradeoffs were previously determined under design definition study - see Ref. 1 sections 2.2.7 and 3.4.

2.1.3 Interface Definition

The following is the specification for the analog/digital interface for the modulator. It describes the switch control signals and D/A converter input.

Sub-Carrier D/A Interface

The sine ROM contents will be as follows:

$$A(n) = 127 \sin \frac{2\pi n}{512}$$

A(n) = Contents of address n (8 bits)
(2's complement code)

n = Address $0 \leq n \leq 511$ (9 bits)

In the case of the sub-carrier synthesizer the ROM will drive the D/A converter directly. The converter represents 1 standard TTL load.

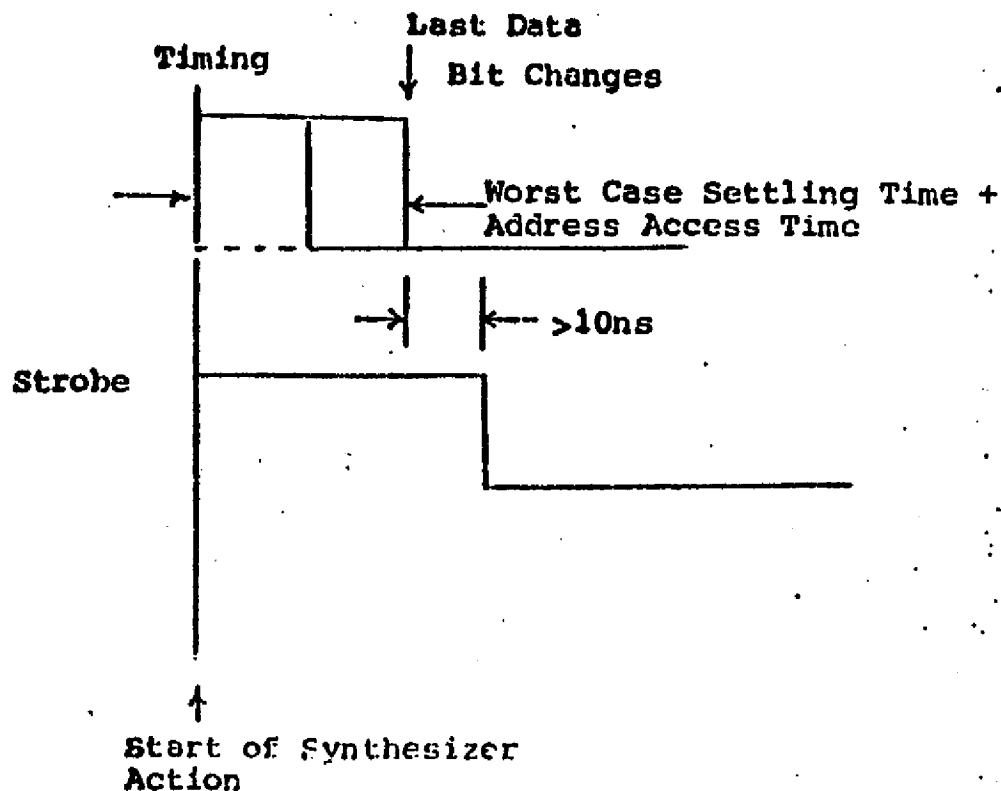
"0" +.5V @ 1.6 ma (sink)
"1" +2.5V @ 50 μ a (source)

At the completion of tone bursts in NASA 3 and 4 and at the completion of all modulation types the last word to the D/A is to be a "zero" (00000000), which is also the contents of memory location zero of the ROM. During power turn-on and then during any time the sub-carrier synthesizer is not used, this same word should be sent to the D/A.

Modulation D/A Interface

The contents of the modulation ROM is the same as that of the sub-carrier ROM. The same conditions concerning the last word to the D/A as in the sub-carrier case apply.

Unlike the sub-carrier D/A the ROM contents must be loaded into a parallel to parallel register to eliminate bad data due to address bit timing problems.



Switch Control Signals

The following signals are required for controlling the various FET switches.

<u>Name</u>	<u>Active State (High)</u>	<u>No. of Loads</u> ⁽¹⁾
N16+	NASA 1 and NASA 6	1
NAS2EN+	NASA 2	3
N345D+	NASA 3, 4 and 5 and DOD1-13	2
N5D+	NASA 5 and DOD1-13	1
HALT+	When no crosslink output is required	2

(1) One load is -

- "1" $\geq 2.5V$ @ $< 100 \mu A$ sink
- "0" $\leq .8V$ @ $< 4 \mu A$ sink

2.1.3 (Interface Definition, Continued)

NASA 1 and NASA 6 Data Input

The NASA 1 and 6 input drives one gate. The signal is called N16DAT+

"1" > 2.5V @ 40 μ a source

"0" \leq .8V @ 1.6 ma sink

Activity Detector Interface

The Activity Detector output (ACERROR+) is high any time an output fault is detected. That is if no output is detected 4 ms after start of modulator action or some output remains 20 ms after the modulator action stops.

ACERROR+ (output)

represents standard TTL output

"1" > 2.5V @ 40 μ a source

"0" \leq .4V @ <16 ma sink

GATE⁻ (input)

represents one standard TTL load

"1" >2.4V @ 50 a (sink)

"0" <.5V @ 1.6 ma (source)

The "GATE" signal from the digital portion of the modulator, provides an indication of when the payload link output should be active.

2.1.4 Modulation Types

NASA 1 (See Figure 2-1)

PCM/BI- \emptyset -L, 8 kB/sec. (8.066 kB/sec.). Each 128-bit command word shall be divided into four 32-bit segments and preceded by a 32-bit frame-sync sequence. When time-multiplexed with digital voice, 128 bits of delta modulated voice data shall be inserted between every 32 bits of command data; the combined information rate is 40 kB/sec. (40,330 kB/sec.). Transmission shall be initiated with a 1 sec. sequence of "ones" in order to establish bit sync. Transmission continues until "stop" instruction received: if no command data available a "null" command shall be transmitted during that interval.

NASA 2 (See Figure 2-2)

A 2 kHz subcarrier shall be 100 percent phase-modulated by the 1 kB/sec. PCM-PSK data and summed with an equal-amplitude 1 kHz sinewave tone. Each transmission shall be initiated with a 1 sec. sequence of "ones" in order to establish bit sync. Multiples of five zeros shall be inserted between command blocks when no data is available. The composite PCM-PSK and summed reference shall frequency modulate a 70 kHz oscillator with a deviation of ± 5 kHz.

NASA 1 MESSAGE FORMAT

WITHOUT
VOICE

9.066 KBITS/SEC
OR
124 μ SEC/BIT

1 SECOND
OF ONES

32 BITS
FRAME
SYNC.

32 BITS
DATA

32 BITS
DATA

32 BITS
DATA

32 BITS
DATA

160 BITS = 19840 μ SEC

128 BIT COMMAND WORD

WITH
VOICE

40.330 KBITS/SEC
OR
24.8 μ SEC/BIT

1 SECOND
OF ONES

32 BITS - FRAME SYNC

128 BITS
VOICE

32 BITS - DATA

128 BITS
VOICE

32 BITS - DATA

128 BITS
VOICE

32 BITS - DATA

128 BITS
VOICE

32 BITS - DATA

128 BITS
VOICE

800 BITS = 19840 μ SEC

ENCODED WAVEFORM IS GENERATED BY MULTIPLYING SQUAREWAVE SUB CARRIER DURING EACH BIT TIME BY +1 (NO CHANGE) FOR A LOGIC ONE OR BY -1 (180° INVERSION) FOR A LOGIC ZERO. 1 BIT TIME = PERIOD OF SQUAREWAVE.

TYPICAL DATA

LOGIC →

1 1 1 0 1 0 0 1

ENCODED
WAVEFORM →

BIT
TIME

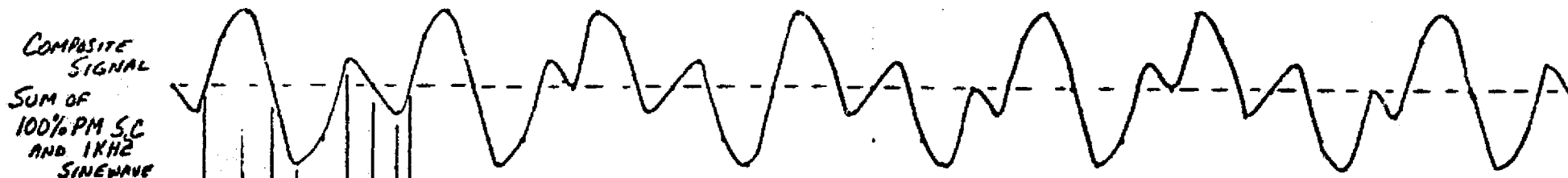
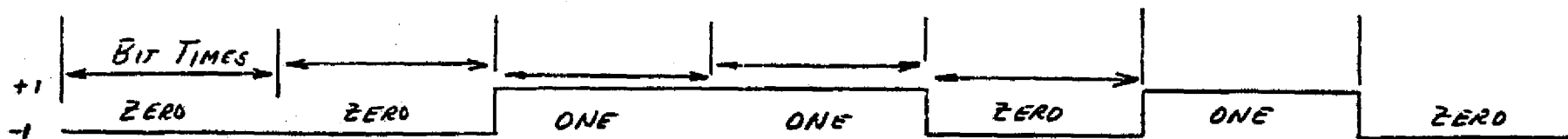
24.8 μ SEC - WITH VOICE

124 μ SEC - WITHOUT VOICE

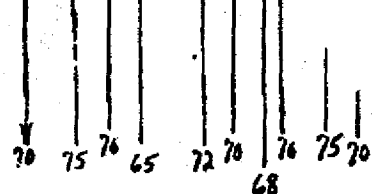
$$\frac{\text{BIT TIME INTERVAL}}{\text{SUB CARRIER PERIOD}} = 1$$

$$\text{I.E. } \frac{\text{SUBCARRIER FREQ}}{\text{DATA RATE}} = 1$$

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2-72
FM MODULATED
5 KHz DEVIATION
ABOUT 70 KHz



NASA 2
GENERATION

OUTPUT FORMAT

1 SECOND OF ONES	3(X5) BITS	3(X5) BITS	[6, 16, 21, 42, 6] (X5) BITS	MULTIPLES OF 5 ZEROS
	VEHICLE ADDRESS	SYSTEM ADDRESS	DATA	

NOTE: EACH "ZERO" VEHICLE ADDRESS BIT SHALL BE REPRESENTED BY A 5 BIT PATTERN - A -, EACH ONE BY A

SIMILARLY EACH ZERO SYSTEM ADDRESS OR DATA BITS IS REPRESENTED BY A 5 BIT PATTERN - B -, EACH ONE BY B

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FIG 2-2

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2.1.4 (Modulation Types, Continued)

NASA 3 (Figure 2-3)

FSK using up to 15 address tones and seven execute tones as

<u>Address Frequency (Hz)</u>	<u>Execute Frequency (Hz)</u>
1025	2000
1097	2270
1174	2650
1262	3000
1352	3305
1447	3621
1549	3850
1750	
1860	
4245	
4550	
5155	
5451	
5790	
6177	

The duration of each tone shall be equal to 0.5ℓ seconds with ℓ an integer in the range $1 \leq \ell \leq 7$; ℓ shall be specified by bits 29-31 of CE Command Instruction Format. The interval between tones shall equal 0.5 seconds, and the interval between messages shall be at least 0.5 seconds.

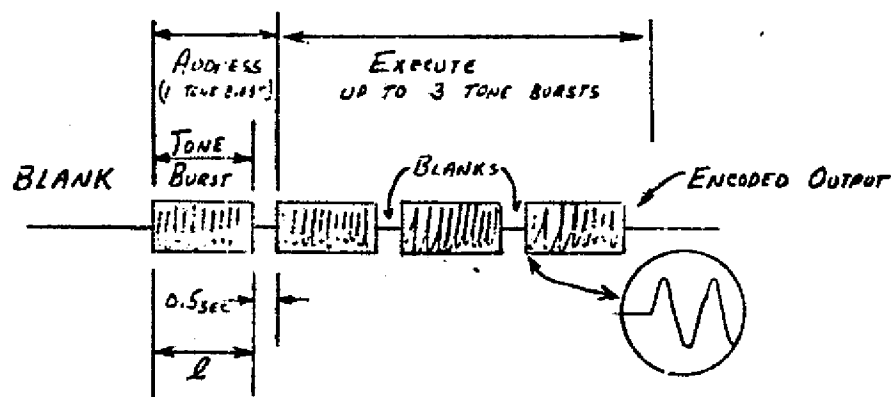
NASA 4 (Figure 2-4)

Four-symbol pulse duration modulation: 75%, 50%, 25% and 0% (representing "sync", "one", "zero", and "blank", respectively). The sub-carrier shall be a fixed tone in the 7000 to 11,024 Hz range. The (100%) pulse train interval shall be defined as 72 sub-carrier cycles. Each address word and each execute word shall be preceded by a "sync" pulse which is in turn preceded by a "blank" pulse. An additional "blank" and "sync" pulse shall be inserted at the end of transmission.

NASA 5 (See Figure 2-5)

Two-tone (using two assigned frequencies in the 7 to 21 KHz band) FSK modulated by the PCM-NRZ data. This modulated signal shall be 50% amplitude modulated by a sinusoidal bit synchronization signal having a period equal to one bit interval. The positive-going zero-crossing of this sync signal shall be specified to occur either at the beginning of each bit interval, or delayed relative to this point by either 1/4 or 1/2 of the bit interval. Allowable bit rates (fixed for each recipient vehicle) in bits/sec: 2^i (i is an integer $3 \leq i \leq 10$) and $100i$ (i an integer $1 \leq i \leq 12$).

NASA 3 MESSAGE FORMAT



4 BITS (0000 NOT USED) DETERMINE WHICH OF 15 ADDRESS TONES IS GENERATED
3 BITS (000 NOT USED) DETERMINES EXECUTE TIME

TURN ON, TURN OFF AND SELECTION OF TONE TO BE A CONTROLLER FUNCTION

DURATION OF BLANK (I.E. NO SIGNAL) = 0.5 SEC. (CONSTANT)

DURATION OF TONE BURST = L WHERE $L = 0.5, 1.0, 1.5, 2.0, 2.5, 3.0$ OR 3.5 SEC (IS SPECIFIED IN BITS 29-31 OF CE COMMAND INSTANTAN)

ADDRESS CONSISTS OF 1 BURST. OF

ONE OF 1025 HZ

THE FOLLOWING: 1097
1174
1262
1352
1447
1549
1750
1860
4250
4350
5155
5451
5790
6177 HZ

EXECUTE CONSISTS OF UP TO 3 TONE BURSTS OF THE FOLLOWING FREQUENCIES

2000 HZ
2270
2650
3000
3305
3621
3850 HZ

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FIG. 2-3

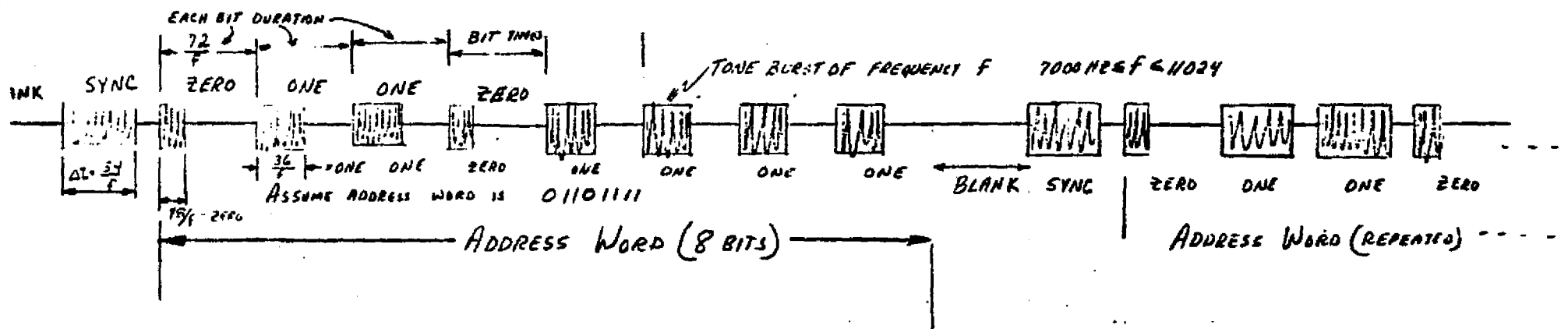
REN:7540

Rev. 1 - 21 Feb

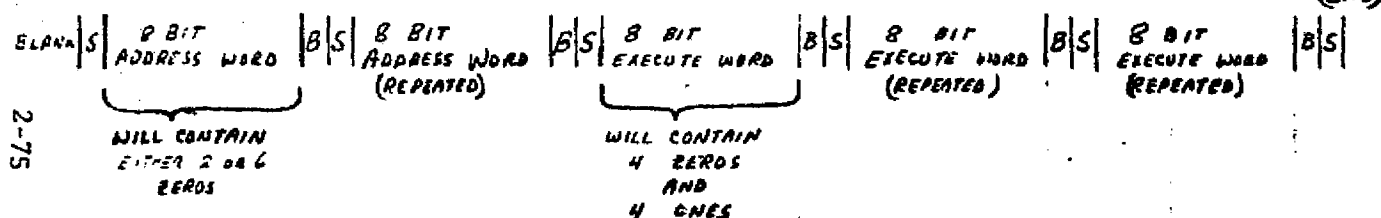
Rev Feb

NASA 4 MESSAGE FORMAT

EXPANDED PORTION OF MESSAGE



COMPLETE MESSAGE IS AS FOLLOWS: B = BLANK, S = SYNC.



SUMMARY:

A. 4 POSSIBLE SYMBOLS TRANSMITTED

1. BLANK - NO SIGNAL
2. SYNC - 54 CYCLES OF SUB CARRIER
3. ONE - 36 CYCLES OF SUB CARRIER
4. ZERO - 18 CYCLES OF SUB CARRIER

B. FREQUENCY OF SUB CARRIER FIXED IN RANGE FROM 7000 HZ TO 11024 HZ

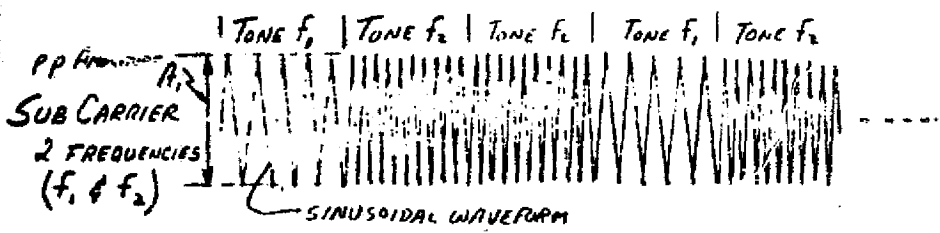
TIME DURATION OF PULSE AND BLANKS.
CONTROLLED BY M & N REGISTERS IN
MODULATOR

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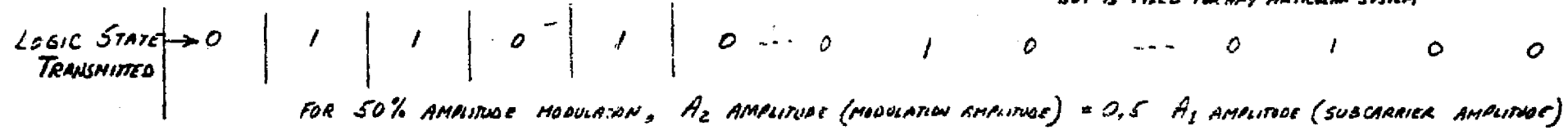
FIG. 2-4

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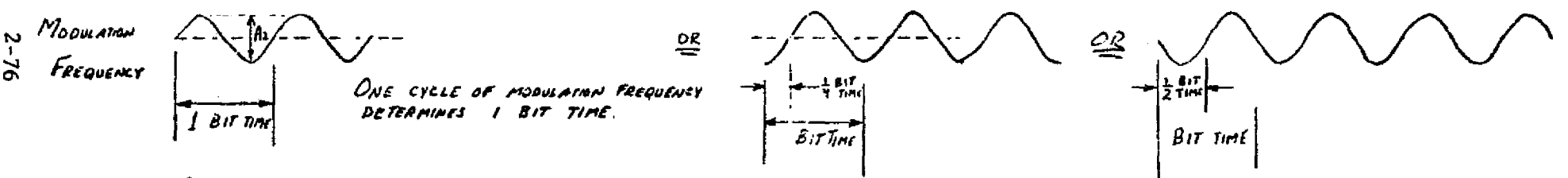
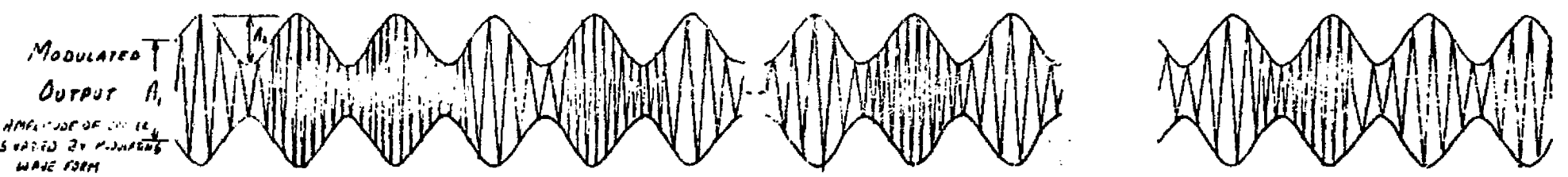
TONE f_1 CORRESPONDS TO A LOGIC 0
TONE f_2 CORRESPONDS TO A LOGIC 1
TWO TONES ASSIGNED IN RANGE FROM 7KHZ TO 21KHZ



COMPLETE NASA 5 COMMAND FORMAT

INITIALIZATION	MESSAGE	TERMINATION
≥ 13 ZEROS	1 7 BITS ADDRESS 8 - n COMMAND	≥ 2.0 ZEROS

WHERE n IS AN INTEGER $7 \leq n \leq 64$
BUT IS FIXED FOR ANY PARTICULAR SYSTEM



DELAY OF POSITIVE GOING, ZERO CROSSOVER OF MODULATION FREQUENCY WITH RESPECT TO BIT TIME MAY BE 0 (COINCIDENT), $\frac{1}{4}$ BIT TIME OR $\frac{1}{2}$ BIT TIME. THIS WILL BE FIXED FOR ANY GIVEN VEHICLE (SYSTEM).

MODULATION FREQUENCIES ALLOWABLE (FIXED FOR EACH PARTICULAR SYSTEM)
ARE 2^k BITS/SEC WHERE k IS AN INTEGER $3 \leq k \leq 10$
AND 100λ BITS/SEC WHERE λ IS AN INTEGER $1 \leq \lambda \leq 12$

NASA 5
MESSAGE FORMAT

FIG 2-5
REV: 7510
Rev 21

(NASA 5 [See Figure 2-5], Continued)

Each transmission shall be initialized by a sequence of 13 (or more) "zeros" followed by a "one" and is terminated by a sequence of (at least) 20 zeros.

NASA 6 (Figure 2-6)

Square wave PSK subcarrier with coherent modulation by PCM-NRZ data. The subcarrier frequency shall be 2^i Hz, with $i = 1$ to 12. The data rate shall be 2^j Hz with $j = 0$ to 11. The subcarrier to data ratio shall be from 2 to 2048.

DOD 1 - 13 (See Figure 2-7)

The three-tone FSK modulated by the PCM-NRZ data shall be either 1 kB/sec or 2 kB/sec. The three tones shall be 95 kHz ("one"), 76 kHz ("zero"), 65 kHz ("S"). The "S" or space symbol is used only when neither a "one" or a "zero" available for transmission. The FSK signal shall be 50% AM modulated by a symmetric triangular wave having a period equal to two bit intervals. The positive-going zero-crossing of the triangular wave shall be delayed from the bit-transition point by 6/10th of a bit interval.

Each transmission shall be initialized by a 1-second interval of "S's" and "S's" are inserted between commands when no data is available.

2.1.5 Block Diagram Description

Figures 2-8 thru 2-12 show the block diagrams of the Analog portion of the modulator with the signal paths highlighted for the various modulation modes.

NASA 1 and 6 (Figure 2-8)

In NASA 1 and 6 the BL-Ø-L data drives an open collector gate that switches the +15 and -15V inputs to produce a ± 1 volt output.

NASA 2 (Figure 2-9)

In NASA 2 the two D/A converters convert the digital output of the modulation synthesizer and subcarrier synthesizer into a 1 kHz and 2 kHz sine wave. These signals are summed in the V/F converter input where they produce a frequency modulated 70 KHz pulse train. A filter at the output of the V/F converter produces a sine wave that is buffered to produce a 2V peak-to-peak output.

NASA 6 (GENERALIZED NASA 1)

in NASA 1 (BI-φ-L), $\frac{\text{BIT TIME}}{\text{PERIOD OF SUB-CARRIER}} = 2^0 = 1$
 in NASA 6:

$$2^1 \leq \frac{\text{BIT TIME}}{\text{PERIOD OF SUB CARRIER}} \leq 2^2 (2048)$$

$$2^1 \leq \text{FREQUENCY OF SUB CARRIER (SQ. WAVE.)} \leq 2^{12} (4096 \text{ Hz})$$

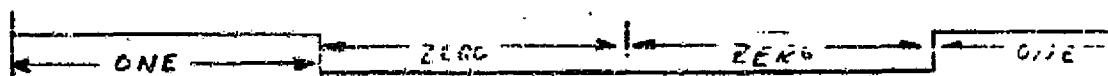
$$2^0 \leq \text{FREQUENCY OF DATA BITS} \leq 2^2 (2048 \text{ Hz})$$

SUB CARRIER



DATA

$$\frac{\text{BIT TIME}}{\text{PERIOD OF S.C.}} = 2^2 = 4$$



ENCODED DATA



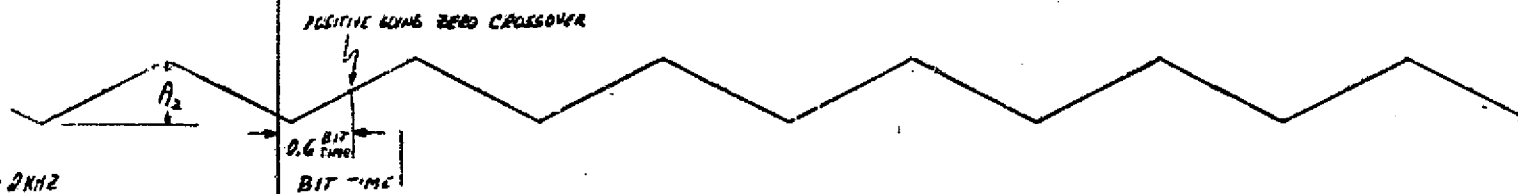
SPACE FREQUENCY = 65 KHZ
 ZERO FREQUENCY = 76 KHZ
 ONE FREQUENCY = 95 KHZ

FREQUENCY OF SUB CARRIER VARIES WITH DESIRED LOGIC STATE (3)



LOGIC STATES | SPACE | SPACE | SPACE | SPACE | SPACE | ONE | ZERO | ONE | SPACE | ZERO | SPACE | ONE |

TRIANGULAR
MODULATION
FREQUENCY
EITHER 1 KHZ OR 2 KHZ

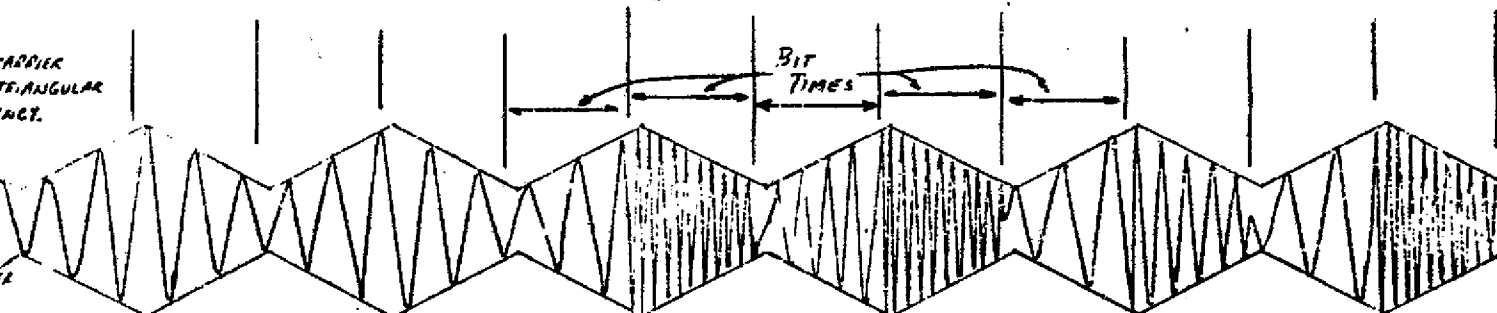


FOR 50% AMPLITUDE MODULATION, A_2 AMPLITUDE = 0.5 A_1 AMPLITUDE

AMPLITUDE OF SUB CARRIER
IS VARIED BY THE TRIANGULAR
MODULATION FREQUENCY.

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MODULATED
OUTPUT
SUM OF SUBCARRIER
AND
TRIANGLE MODULATION
FREQUENCIES



DOD 1-13
GENERATION

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FIG. 2-7

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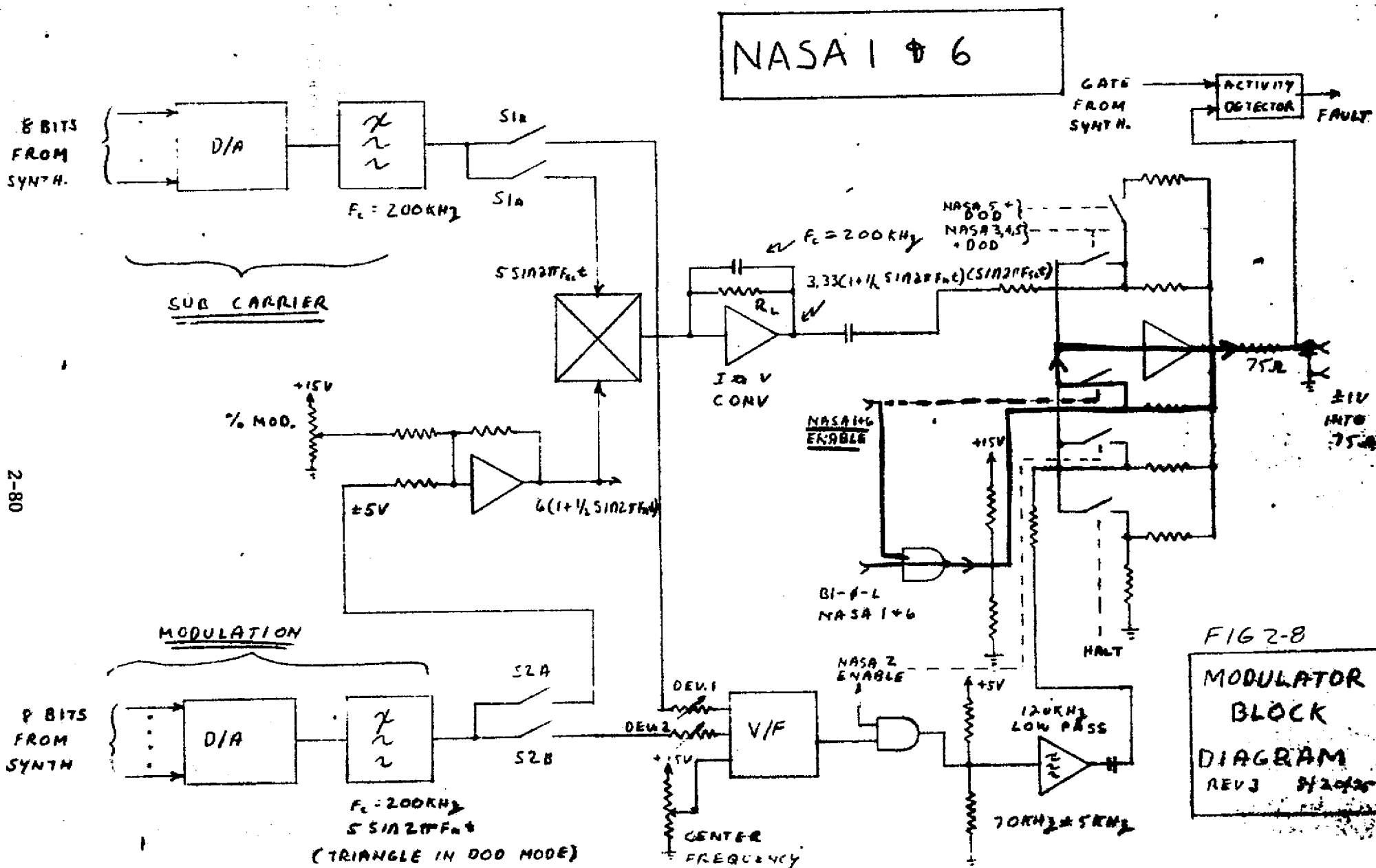
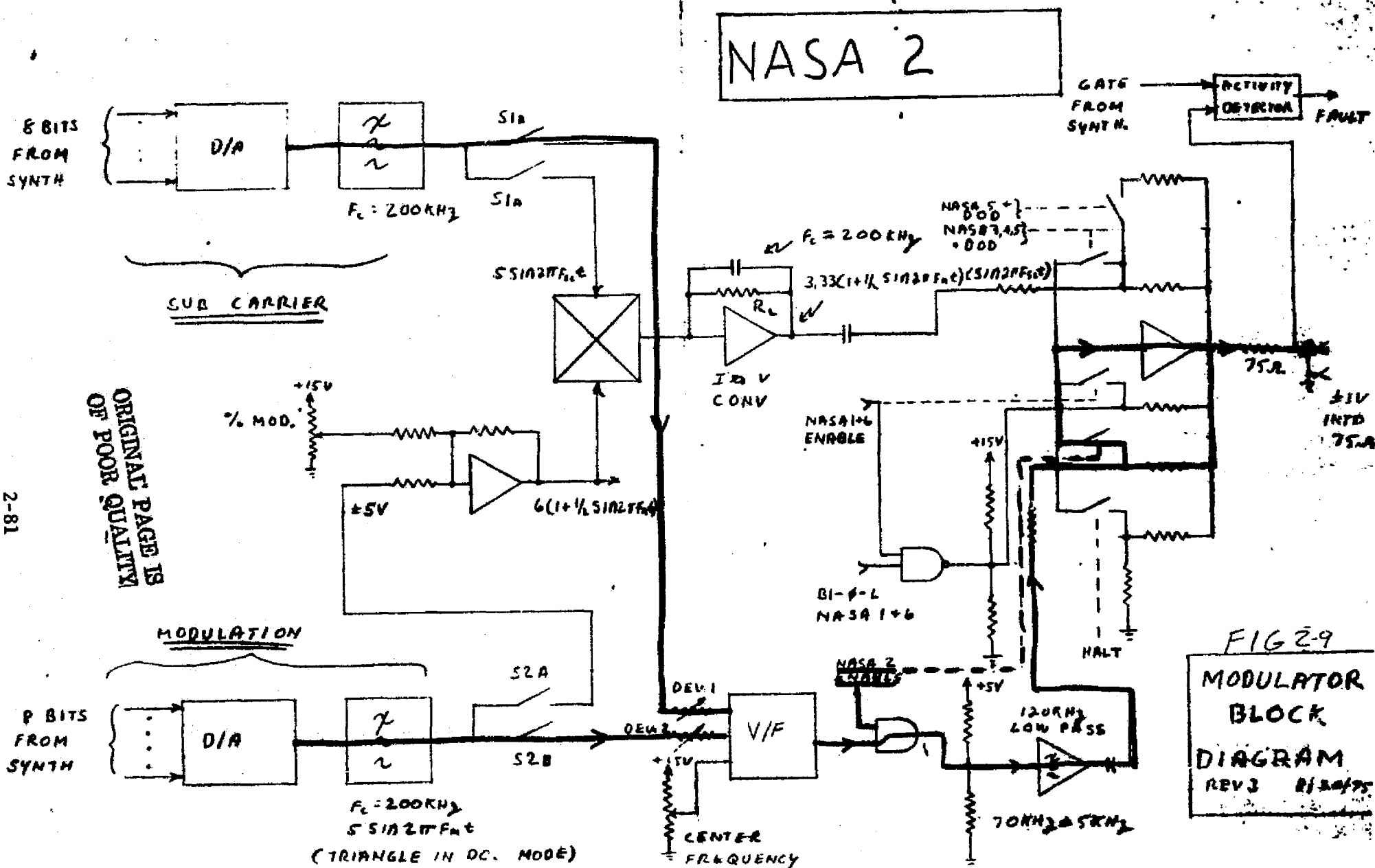


FIG 2-8
MODULATOR
BLOCK
DIAGRAM
REV 3 5/24/20



NASA 3 and 4 (Figure 2-10)

The digital representation of the tone bursts are converted to an Analog signal by the subcarrier D/A. This signal is one input to the multiplier, the other is a constant as determined by the summing amplifier and the fact that in this mode no modulator D/A output is sent to the summing amplifier. The output of the modulator is converted to a voltage by the I/V converter and then buffered to 2V peak-to-peak for the cross-link output.

NASA 5 (Figure 2-11)

The subcarrier is converted to an analog signal by the D/A and is one input to the multiplier. The modulation digital signal is converted to an analog signal in the modulation D/A but is summed with a constant in the summing amplifier so that A M modulation function may be realized in the multiplier. That is, the output of the multiplier is

$$\text{SIN } 2\pi F_{\text{SC}} t (1 + 1/2 \text{ XIN} 2\pi F_{\text{M}} t)$$

F_{SC} = subcarrier frequency

F_{M} = modulation frequency

The multiplier output is converted to a voltage by the I/V convertor and then buffered to 2V peak-to-peak for the cross-link output.

DOD 1-13 (Figure 2-12)

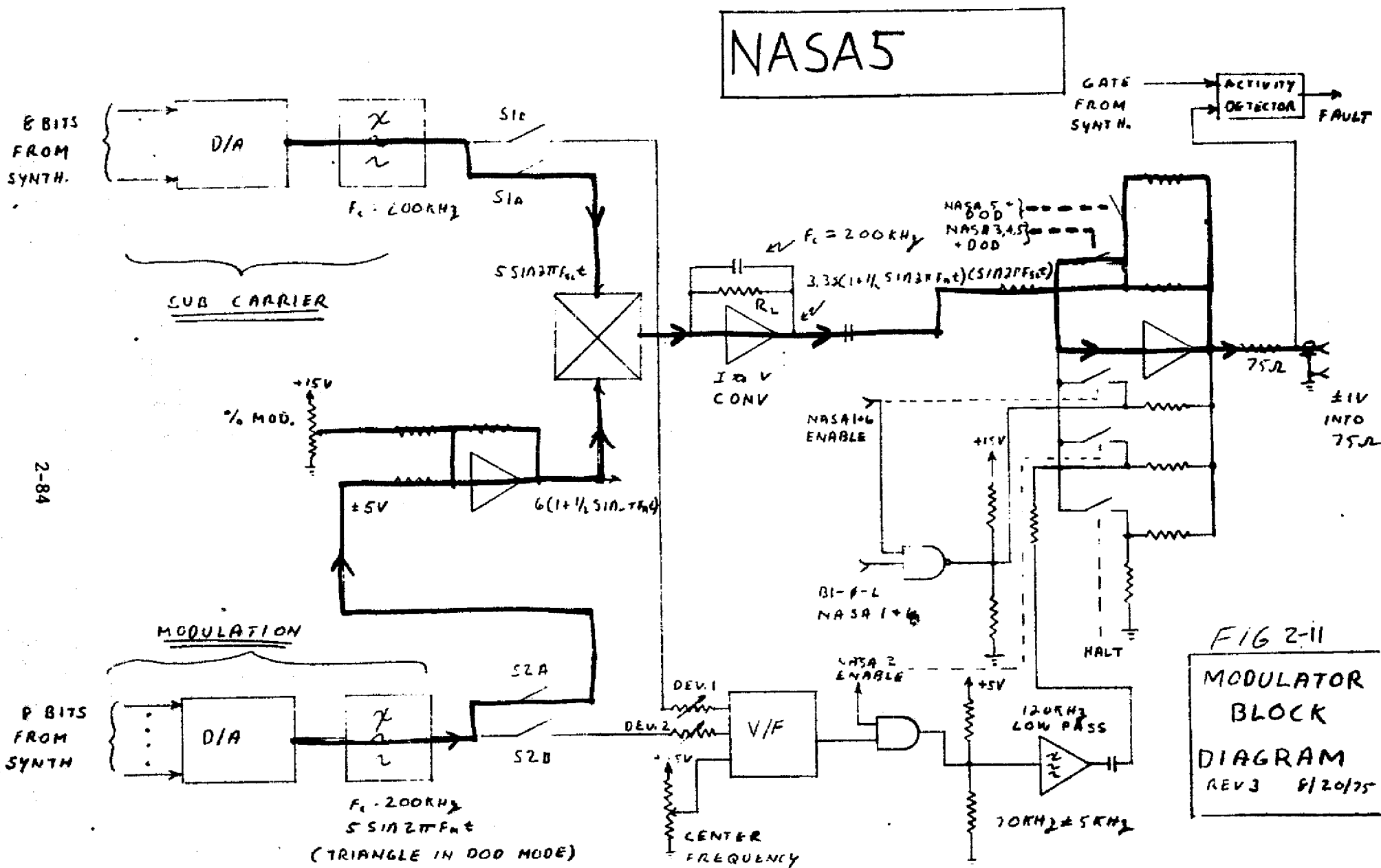
The DOD 1-13 generation is the same as that above in NASA 5 except that the modulation convertor receives a digital representation of a triangular waveform instead of a sinewave as in NASA 5.

Halt (Figure 13)

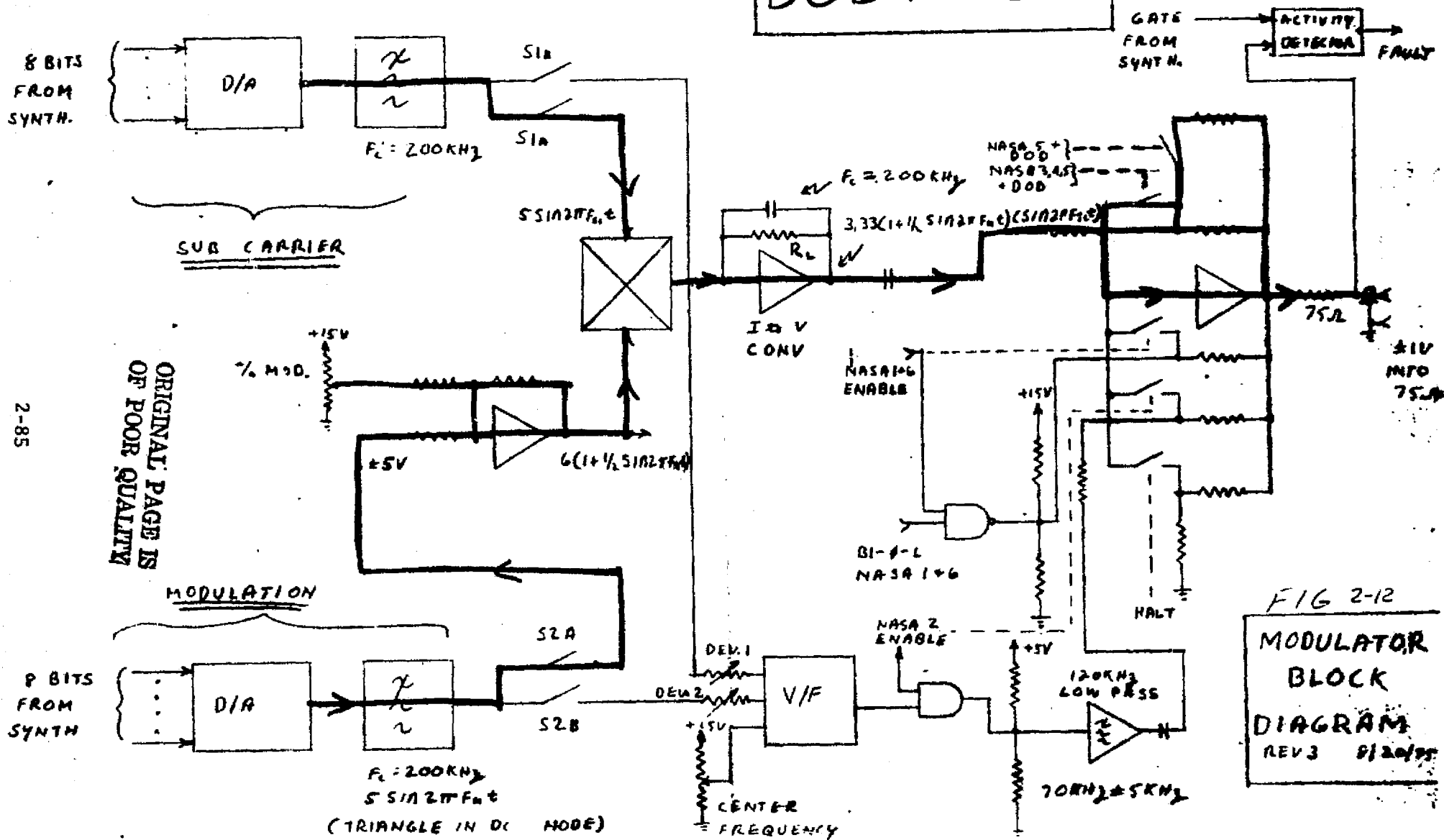
This mode prevents any noise from appearing on the crosslink when the encoder is not running. It also prevents the output amplifier offsets from driving the crosslink to the op-amp limits. For this mode the LM318 is connected as an amplifier with a gain of 1 with 0 V input. The signal HALT also controls the reference input for all the other FET switches so that none of these may be closed when HALT is active. This prevents the switching transients of the digital portion from showing on the output.

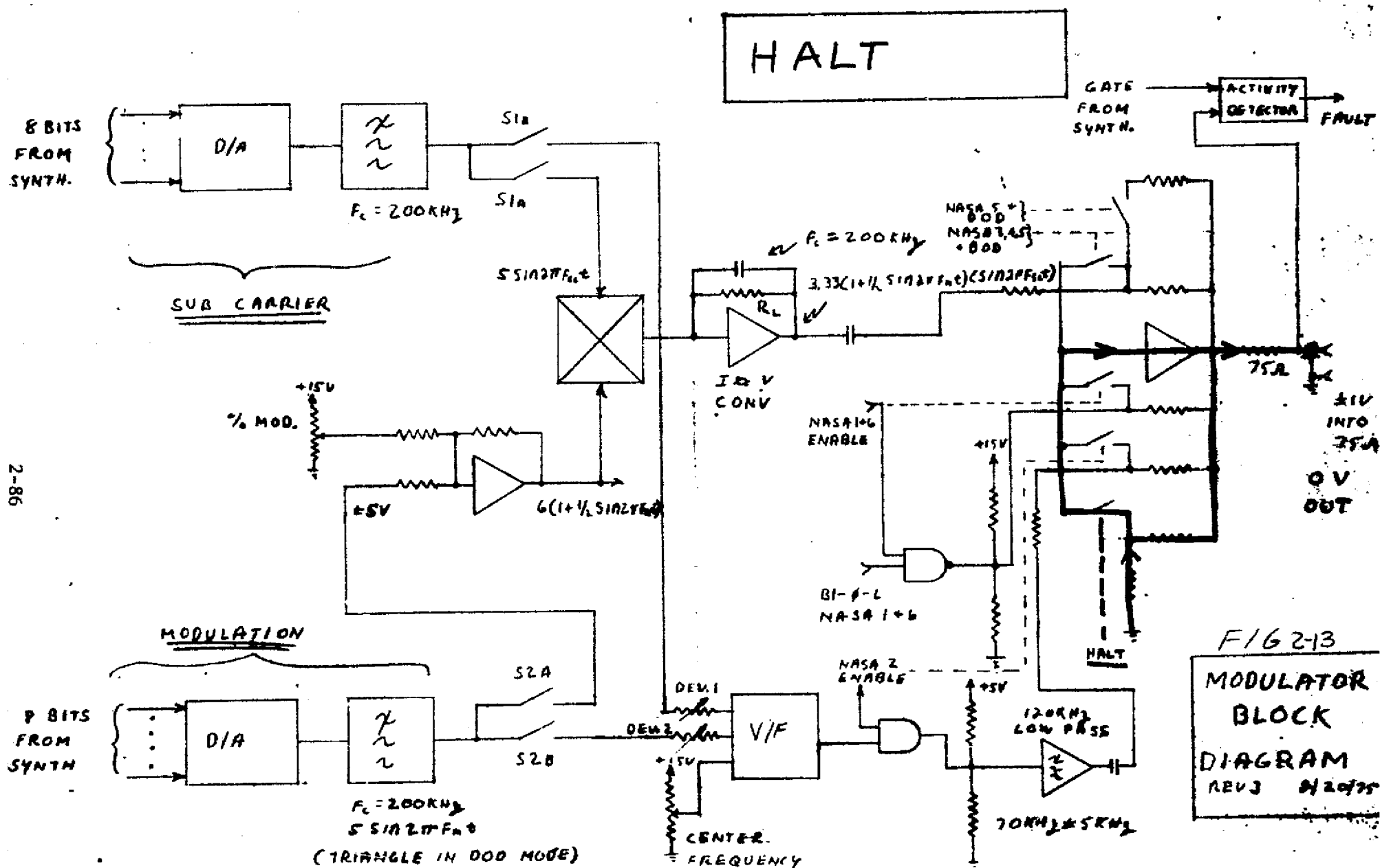
2.2 Design Approach

The generalities of the design of the modulator were determined during the Encoder Design Definition Study so that the task here is a detail design. Therefore, only design details are discussed here. A discussion of the design approach is given in Ref. 1, Section 3.4.



DOD 1-13





2.3 Detail Description

2.3.1 Output Amplifier

The purpose of this amplifier is to provide the $\pm 1V$ output into 75 ohms for the various modulation types. The basic configuration used in all modes is shown in Figure 14 which is a basic amplifier with a 75 ohm source impedance and gain less than 1. An LM318 was used for its current capability of up to 20 ma, its wide bandwidth and high slew rate for preserving the rise time and keeping the jitter low in the NASA 1 and 6 modes. It is also short circuit protected.

The switches are DG151 selected for the low on resistance and low feed-through at high frequencies when off. They are connected between the summing junction of the gain network and the input of the amplifier so as to eliminate the FET on resistance from influencing the gain of the amplifier. No current will flow through the FET so as its own resistance changes with age and temperature it does not affect the gain.

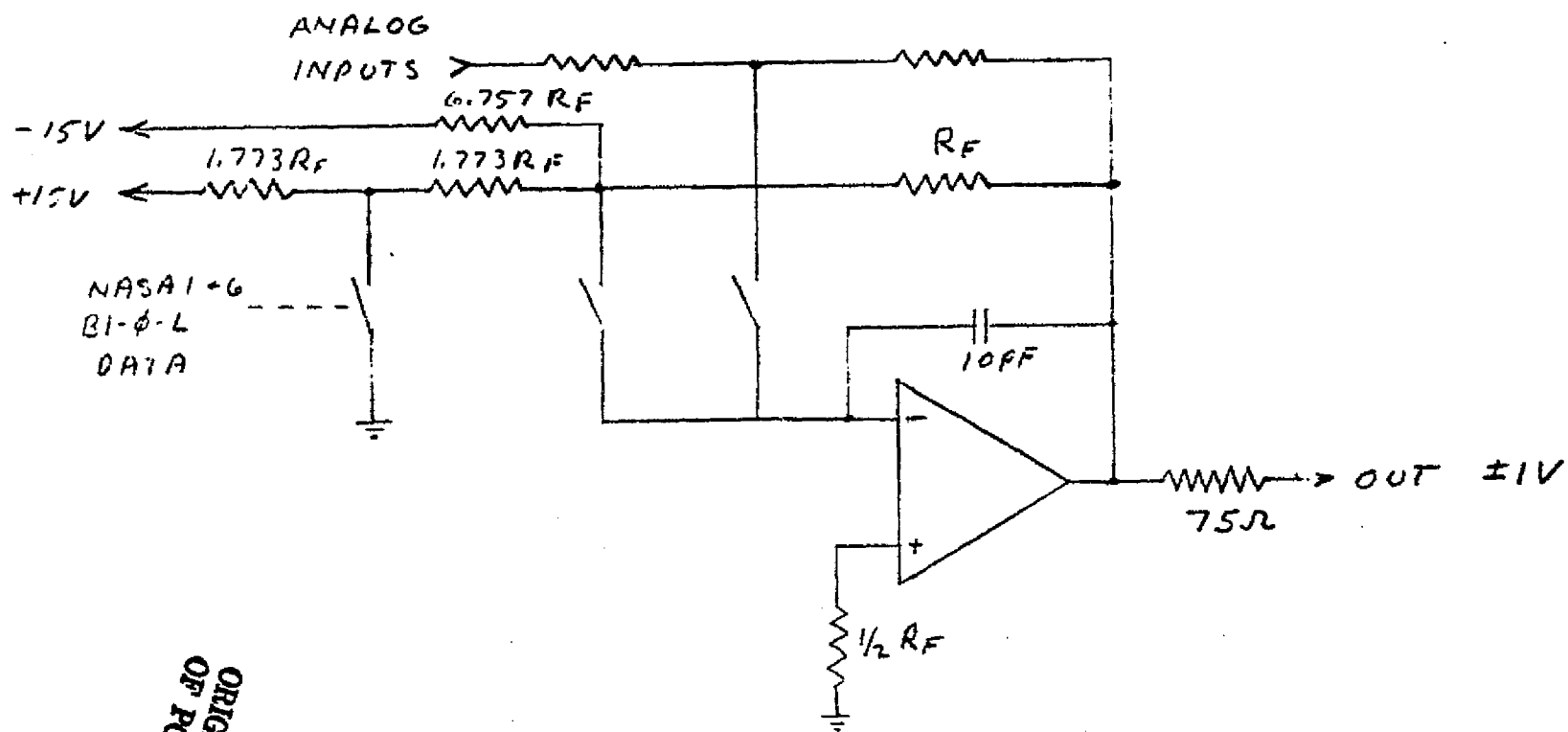
The NASA 1 and 6 $\pm 1V$ waveform is produced by summing a -15V signal with a 0 volt input for a +1V output or summing the -15V with +15V to produce a -1V output. An open collector nand gate, 74L03, is used for switching the 0V and +15V. This is also shown in Figure 2-14.

2.3.2 Multiplier

The multiplier is a conventional application of the Motorola MC1594. The scale factor resistors and load resistors in the I/V convertor have been chosen for a gain of 9 so the output voltage is 5 volts peak. Two 20K ohm pots are used for adjusting the voltage offset of the X and Y inputs. These are necessary for proper alignment of the modulation feedthrough. An LM318 is used as a current to voltage convertor at the output of the multiplier. A capacitor is used across the load resistor to insure stability and also decrease the response above 200 KHz. It has a breakpoint at 340 KHz and at 100 KHz, the highest frequency required at the output of the multiplier, the response is down -.36 dB.

2.3.3 Summing Amplifier

This is an LM318 in a conventional summing amplifier mode. It sums the modulation with a constant so as to produce the AM signal in the multiplier. It also supplies a D.C. input to the multiplier to feed the sub-carrier straight thru the multiplier in the tone burst modes. The constant 8 volt input is generated by a zener for stability and is adjustable so that the modulation depth can be varied in NASA 5 and DOD modes.



OUTPUT AMPLIFIER
SIMPLIFIED

FIG. 2-14

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2.3.4 V/F Convertor

This supplies the FM modulated 70KHz for the NASA 2 mode. The outputs of the subcarrier and modulation D/A convertor are summed at the current input of the voltage to frequency convertor and then summed with an offset voltage at the voltage input. This way the center frequency is determined by the offset voltage and the subcarrier and modulation signals produce the ± 5 KHz deviation. The output of the V/F convertor is a 70KHz train of 7 microsec. pulses. These drive a 70KHz tuned circuit and 100KHz lowpass filter so as to produce a sinusoidal signal. This low pass filter is a simple two pole active filter using an LM318, which also supplies gain. By way of the FET switch, this signal is buffered by the output amplifier for the crosslink output.

The center frequency and the deviation of the V/F are controlled by 3 pots. The 2 pots for the deviation may be replaced with fixed resistors after debug as they are actually a nominal dependent on the gain of previous stages. However, the center frequency adjustment will always remain a pot for convenience of changing the center frequency.

2.3.5 D/A Convertors and Filters

This circuitry provides the conversion of the digital representation of the subcarrier and modulation waveforms from the synthesizers to analog signals. Both D/A's are bipolar with a ± 10 V output and use a 2's complement code on the input. Each D/A has a filter on its output to eliminate aliasing. With a sampling rate 8 times the highest frequency to be generated the filtering task is not very difficult, so simple RC filters are used. An ECAP plot of their response is shown in Figure 2-15. Depending on the response of the circuitry following these filters, their breakpoints may have to be moved to a higher frequency at debug.

Due to the fact that some bits of the modulator word travel different paths in the synthesizer, some bit-to-bit skew could result that would generate noise on the D/A output. To eliminate this the data is strobed into a register of two 74L95's to whose outputs the D/A is connected.

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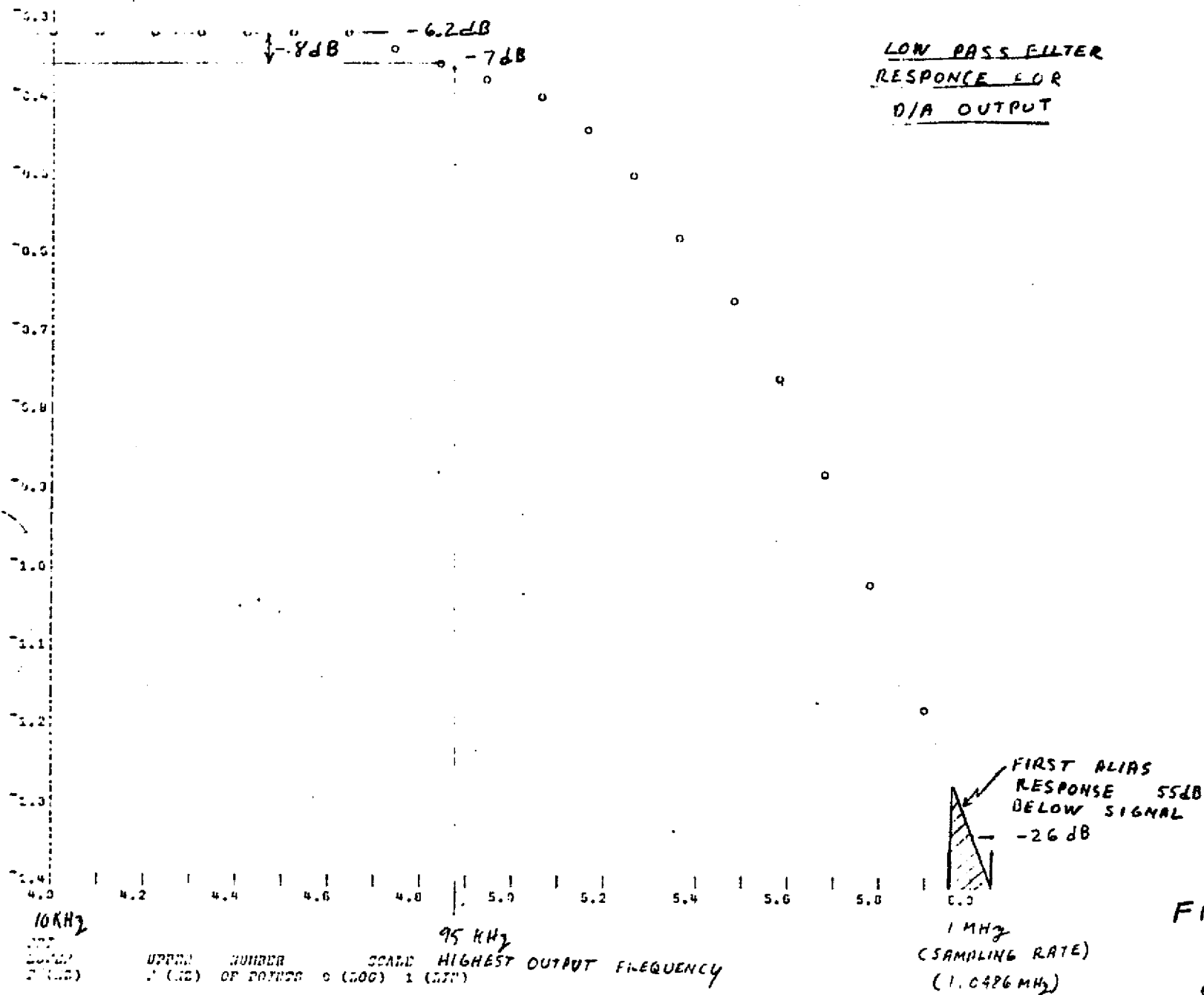


FIG. 2-15

SAMPLING FUNC. RESPONSE - 35dB AT
FIRST ALIAS, -75-20 = -55dB

2.3.6 Activity Detector

The only BITE for the analog portion is contained in the activity detector. This monitors the crosslink output and signals the digital portion of the modulator if there is any output when the modulator should be halted or there is no output when it should be running. Figure 2-16 is a block diagram of the detector. The first stage provides a gain of 5 and drives a full wave detector. This charges an RC circuit with a fast charge, slow decay time-constants thus providing filtering and fast response at low frequencies. When the charge exceeds 4 volts the voltage comparator triggers. This comparator uses positive feedback to provide hysteresis so as to minimize the effect of ripple. The comparator output is compared to the gate signal from the digital portion of the modulator for errors. To prevent false errors on the start and stop of a modulator action due to the slow charge and discharge of the RC filter, two one shots shut off the comparator for these periods of time.

2.3.7 Oscillator

This provides the 2^{22} Hz for the synthesizer. It has been placed in this portion of the modulator since its .4 inch height is too large for the digital boards.

2.4 Schematics

<u>Drawing No.</u>	<u>Title</u>
893204	Modulator Analog No. 1
893205	Modulator Analog No. 2

2.5 Test Results

The results of tests of the modulator signal characteristics are shown in Table 1. These specifications are from the sales order or from those discussed above in Section 2-1. The test procedure gives the information that is loaded into the digital portion of the modulator by the microcontroller through the local control panel. An LCP was available for this testing. A list of test equipment used follows:

1. Tektronix 545B with 1A4 vertical plug-in and X10 probe, P6028
2. Hewlett-Packard 5248L Counter
3. Hewlett-Packard 334A Distortion Analyzer

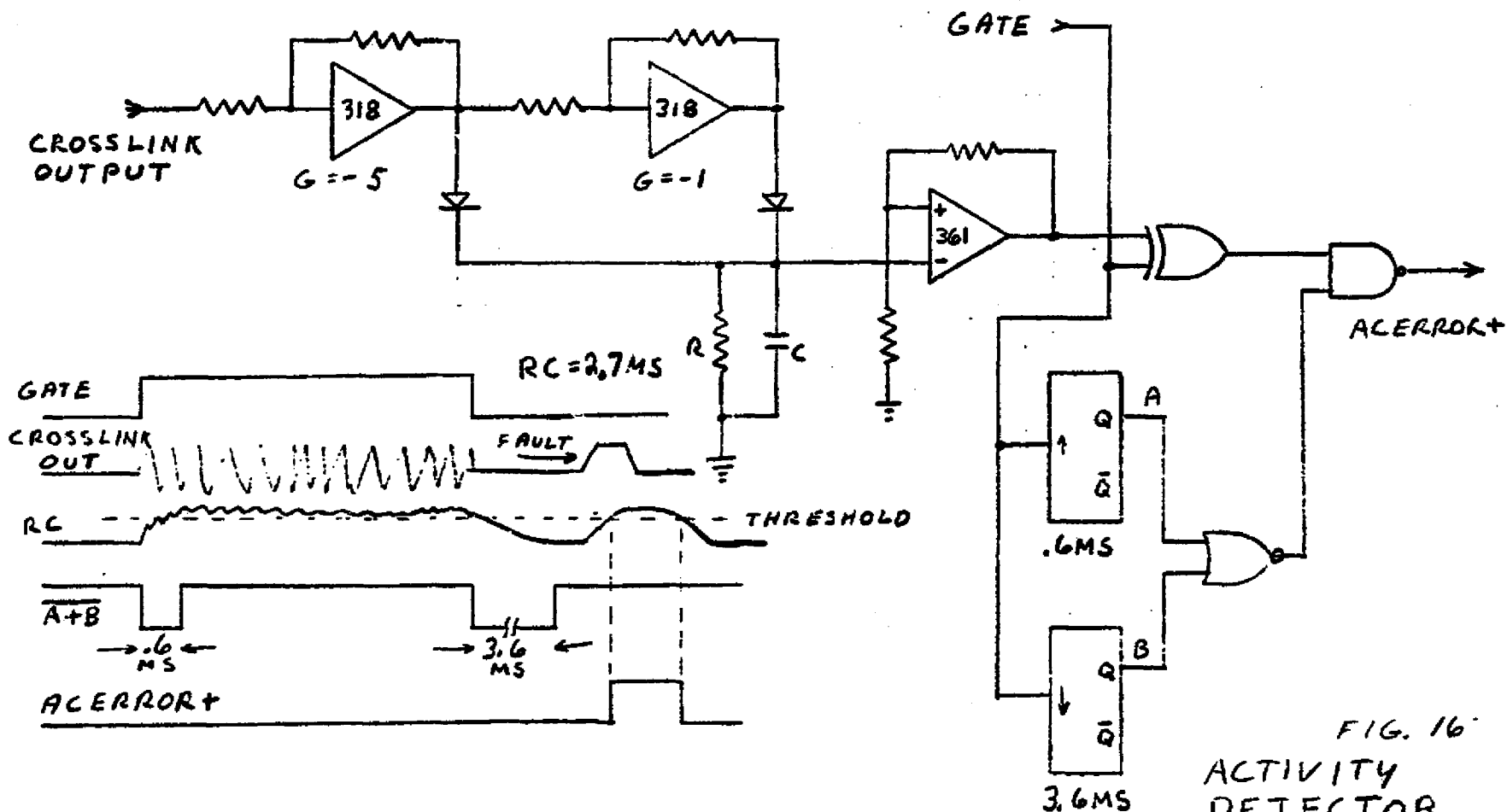
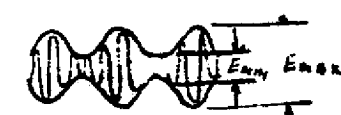


FIG. 16
ACTIVITY
DETECTOR,
BITE

CROSSLINK OUTPUT PERFORMANCE

TEST NO.	PARAMETER	CODE	TEST PROCEDURE				OBSERVATION POINT	SPEC	VALUE MEASURED	ADJUSTMENT	REMARKS	(S.O. 81364 PARA. NO.)
			REGISTER	ADDRESS	DATA							
1	BI-Φ-L OUTPUT VOLTAGE	NASA 1+6	F ₂	74101	000000 0 Hz	CROSS-LINK	CROSS-LINK	1V TERA	±105V	R6+R7 CE04	①*	
			F _m	74102	017602 8.00000			±1.1V (±10%)				3.3A
			COUNTER	174103	010010 M=0N=16			<1 μSEC	.65 μA	C5	① LARGER SLOWER RISE TIME, BUT EFFECTS FREQUENCY RESPONSE	
	RISETIME		CONTROL	16100	100000 RUN			RISE-FALL TIME	.65 μA	CE04		3.3.4
								8066 Hz	80660 Hz	NONE	③	
	FREQUENCY							±.005% ±.4 Hz				3.2, 30.1
	JITTER							<5 NS	NONE	NONE	①	
	OSCILLATOR FREQUENCY	ALL					CE01 OUTPUT PIN 39	22 Hz 4.19433 MHz ±.001% ± 42 Hz	4.19433 MHz	NONE	② DETERMINES ALL OUTPUT FREQUENCIES EXCEPT 70 MHz	
3	SUBCARRIER + MODULATOR DIA SCALE FACTOR	5	F _S	174101	16100 400 Hz		T.P.1	10 V _{p-p}	10 V _{p-p}	R1	①	
			F _m	174102	003720 2 Hz							
			COUNTER	174103	000401 M=N=1		T.P.2	6 V _{p-p}	6 V _{p-p}	R2		
			CONTROL	174100	010040 RUN							
4	SUBCARRIER MULTIPLIER LINEARITY	5 DOD	(SAME AS 3 ABOVE)				CROSS-LINK	NULL (0V)	0V	R8	① GROUND PIN ES-10 ADJUST R7 FOR NO OUTPUT	
5	MODULATOR MULTIPLIER LINEARITY	5 DOD	(SAME AS 3 ABOVE)				"	NULL (0V)	0V	R7	① GROUND PIN ES-9 ADJUST R7 FOR NO OUTPUT	
6	% MOD	5 DOD	(SAME AS 3 ABOVE)				"	50% E _{MAX} = 3E _{MIN}	50%	R3	① 	$\% \text{ MOD} = \frac{E_{\text{MAX}} - E_{\text{MIN}}}{E_{\text{MAX}} + E_{\text{MIN}}}$

* SEE TEST PROCEDURE LIST

TABLE 1, Sheet 1 of 2

CROSSLINK OUTPUT PERFORMANCE

TEST NO	PARAMETER	CODE	TEST PROCEDURE			OBSERVATION POINT	SPEC	VALUE MEASURED	ADJUSTMENT	REMARKS	(5081364 PARA. NO)
			REGISTER	ADDRESS	DATA						
7	70KHZ CENTER FREQ.	NASA 2	FS	176101	000000 0HZ	CROSS-LINK	70KHZ	70.01 KHZ	R6	①	
			FM	176102	000000 0HZ		±1%				
			COUNTER	176103	002405 M=2, N=5		±700HZ				
			CONTROL	176100	040040						
8	MODULATION DEVIATION	NASA 2	FS	176101	000000 0HZ	"	±2.5KHZ	±2.5KHZ	R5	② SET COUNTER TO .1 SEC SAMPLES AND ADJUST FOR PEAK FREQS. OF 72.5 KHZ AND 67.5 KHZ	3.2, 20.2
			FM	176102	000001 1HZ		±1%				
			COUNTER	176103	002405						
			CONTROL	176100	040040						3.2, 20.2
9	SUBCARRIER DEVIATION	NASA 2	FS	176101	000001 0HZ	"	±50KHZ	±2.5 KHZ	R5	② SAME AS TEST 8	
			FM	176102	000001 1HZ		±1%				
			COUNTER	176103	002405						3.2, 20.2
			CONTROL	176100	040040						
10	NASA 2 OUTPUT	NASA 2	FS	176101	003720 2KHZ	"	2VP-P	2.0V P-P	CE04	①	
			FM	176102	001750 1KHZ		±10%		R2		
			COUNTER	176103	002405		±.2VP-P				3.7.4
			CONTROL	176100	040040						
11	SUBCARRIER FREQUENCY RESPONSE 1KHZ	ALL	FS	176101	001750 1KHZ	"	2VP-P	2.0V Vp-P	NONE	① ③	
			FM	176102	000000 0HZ		±10%				
			COUNTER	176103	001001 M=2, N=1		±.2VP-P	±.7%			
			CONTROL	176100	020040 NASA 3		±5% QIST				
12	"	"	FS	176101	001750 65KHZ	"	2VP-P	2.0V Vp-P	NONE	① ③	
			FM	176102	000000 0HZ		±10%				
			COUNTER	176103	001001 M=2, N=1		±.2VP-P				
			CONTROL	176100	020040 NASA 3		±5% QIST	3.1%			
13	65KHZ OUTPUT	NASA 3+4	FS	176101	005670 3KHZ	"	2VP-P	2.08V P-P	CE04	①	
			FM	176102	000000 0HZ		±10%		R4		
			COUNTER	176103	001001 M=2, N=1		±.2VP-P				
			CONTROL	176100	020040						
14	OUTPUT	NASA 5 000	FS	176101	116100 40KHZ	"	2VP-P	2.0V P-P	CE04	①	
			FM	176102	002000 1KHZ		±10%		R42		
			COUNTER	176103	010020 M=2, N=1		±.2VP-P				
			CONTROL	176100	010040						

2.5.1 Activity Detector

The activity detector detects open or shorts and other failures of the crosslink output on all codes except NASA 5. In this code the detector faults during normal operation when the modulation frequency is below 32 Hz. If the detection threshold is lowered or the filter decay time constant is increased this will not happen. Both of these changes would allow the signal to stay above the lower error threshold during the valleys of the amplitude modulation.

However, if either change is made normal operation of NASA 4 will cause faults. This will happen since then the time for the signal at the filter to decay below the threshold is longer than the 4.8 MS between the sync bursts in NASA 4. Since this is only a problem on 3 of the NASA 5 frequencies the change was not made and the NASA 4 operation remains normal. During NASA 5 operation the activity detector is not enabled by the software. That is, bit 3 of the modulator control word is zero.

3.0 VOICE AND ENCRYPTER INTERFACE MODULE

3.1 Introduction

This document describes the design and implementation of the Digital Voice Interface and Encrypter Interface module required in the Command Encoder.

3.1.1 Digital Voice Interface

The Digital Voice Interface is required to assemble the serial delta modulated voice information into 16-bit words for further processing by the microprocessor (uP).

3.1.2 Encrypter Interface

The function of the Encrypter Interface is to provide double bit input/output buffering between the uP and COMSEC-furnished Encrypter.

3.2 Digital Voice Interface

3.2.1 General Description

The function of the digital voice channel is to assemble the serial delta modulated voice information into 16-bit words for further processing by the Microprocessor (uP). As shown in Figure 3-1, the channel is comprised of a 16-bit serial-to-parallel converter, a 16-bit output register and control logic. Channel operation is initiated by setting a control bit in the modulator which in turn enables the 32 kHz clock. Subsequently, every 500 us. thereafter an interrupt is generated to indicate that the output register is full and ready for use by the uP. The interface continues running as long as the modulator control bit is set.

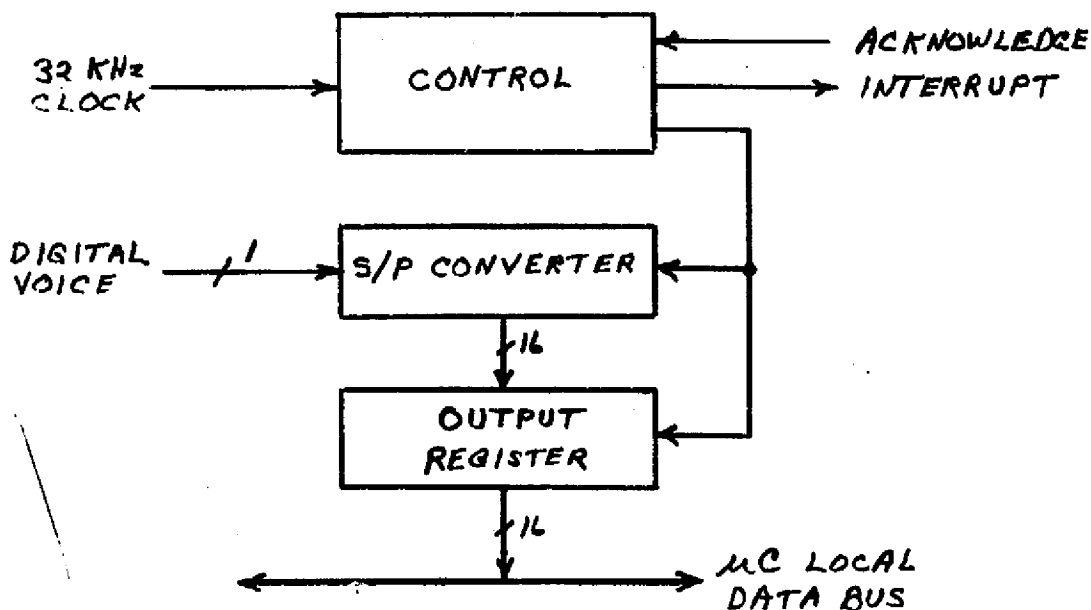


FIG. 3-1

DIGITAL VOICE INTERFACE

3.2.2 Digital Voice Interface Detailed Description

The digital voice interface logic shown in Figure 3-2 consists of a serial to parallel (S/P) converter, an output register, control and μ P interface logic.

Input Sequence

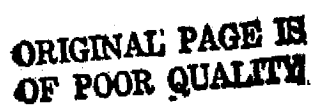
On the leading edge of each clock pulse (32 kHz) issued from the modulator, the logical value of the digital voice input is strobed into the first of two 8-bit shift registers and the 4-bit counter is incremented. At the sixteenth input clock, the carry-out signal from the 4-bit counter sets the Voice Interrupt and the load clock flop. The load output buffer register signal is enabled by the voice interrupt flop output.

On the leading edge of the next clock pulse, the Load CLK flop is reset, clocking the shift register data into the output registers.

Output Sequence

In response to the voice interrupt, the μ P will initiate a read instruction from memory address 176046. The address decode and control logic in conjunction with the μ C CBRQS-signal, enables the data bus drivers and generates a CBACK-signal to indicate valid bus data.

RKA:75:03
13 May 1975
Page 6



2-97

Built-In Test Equipment (BITE)

A test mode is available to aid in debug and fault isolation of the voice interface logic. When the μP issues a CBRQS-signal to address 176045, the V test flop is set. The V test-signal from this flop enables the last stage of the 16-bit shift register to be clocked into the first stage, and disables the normal voice data input. If the shift registers are first cleared, then allowed to shift in the test mode, the output can be checked for bit pick-up. Similarly, the test mode could be entered without a previous clear signal, allowing a fixed pattern to be recycled through the registers and read-out.

Clear Function

The voice interface logic can be cleared either by a programmed clear to memory address 176047, or by the master clear control line signal (MSTCL-).

Bus Interface and Control

The data bus interface is tri-state, operating at standard 54/74 series TTL voltage levels. Bus drivers are held in the high impedance state until a μP fetch operation from location 176046 is issued and decoded. Drivers are National tri-state inverting buffers, DM8098.

Bus activity is controlled by a Request (CBRQS-) signal from the μP and an Acknowledgement (CBHACK-) signal returned from the module. The Request line initiates a bus cycle, while the Acknowledgement line signifies the completion of the response: For a load operation, the transition of the Request line from high to low indicates a valid address and data. The transition of the Acknowledgement from high to low indicates that the data has been accepted.

For a read operation, the transition of the Request line again indicates a valid address. The transition of the Acknowledgement signal from high to low signifies that valid data is available to the μP .

Voice Data and Clock Interface

The digital voice interface with the delta voice modulator shall consist of a serial input data port and a gated output clock for synchronization. When the modulator is set up for digital voice multiplexing, the 32 kHz square wave clock is enabled and sent out to the digital voice modulator. The leading edge is to be used by the modulator to update its output data and the trailing edge is used as a strobe within the digital voice buffer (See Figure 3-3).

Digital Voice Data

The Command Encoder shall accept digital voice data over a twisted pair cable with the following characteristics:

(Digital Voice Data, Continued)

AMPLITUDE

- Logic "0": 0.0 volts \pm 0.5 volts

Logic "1": 5.0 volts \pm 1.0 volts

RISE TIME

- less than 1 usec.

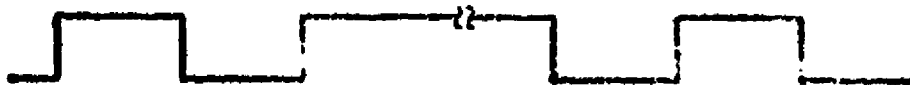
32 KHz Clock

The Command Encoder shall output a gated clock with the following characteristics:

32KHZ CLOCK



DATA IN



BUFFER STROBE TIME



FIG. 3-3

DIGITAL VOICE TIMING DIAGRAM

Frequency

- 32.264 KHz \pm 0.005%

AMPLITUDE

- Logic "0": 0.0 volts \pm 0.5 volts

- Logic "1": 5.0 volts \pm 1.0 volts

DUTY CYCLE
(When Enabled)

- 50 percent \pm 10 percent jitter

RISE TIME

- Less than 150 nanosec.

(Digital Voice Data, Continued)

Twisted pair interface lines are utilized for the interface, with differential line driver and receiver combinations.

3.3 Encrypter Interface

The Encrypter interface logic basically provides single bit input/output buffering between the μ P and COMSEC-furnished Encrypter. The hardware consists of a double-buffered two bit input register, a two bit output register and minimal control logic (See Figure 3-4).

Bit timing and synchronization are derived from the modulator interrupt. The leading edge of the first modulator interrupt samples the input register and if valid, its contents are sent to the encrypter. The next modulator interrupt likewise looks at the input register, etc., but it also issues a clock pulse to the encrypter and strobes the encoded bit into the output register. No interrupt is generated by the encrypter interface since it would be redundant. When employed the encrypter operation overlaps that of the modulator.

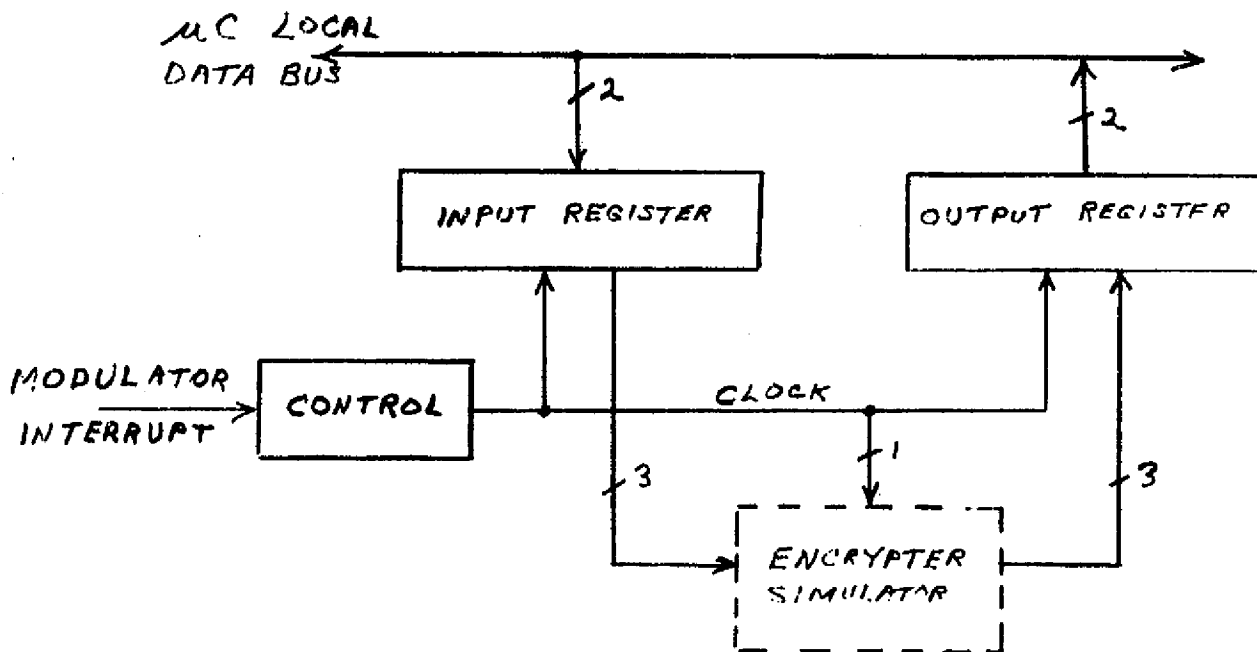


Figure 3-4

Encrypter Interface

3.3.1 Encrypter Interface Detailed Description

The detailed block diagram for the Encrypter Interface logic is shown in Figure 3-5. Operation is initiated by issuing a store instruction to memory location 176040 which sets the valid flop and strobes bits 16 and 15 of the μ P local data bus into the tag buffer and data buffer, respectively. When the next modulator interrupt becomes active, a control signal is generated which transfers the contents of the two input registers and valid flop into the buffer register and resets the valid flop. The tag bit effectively declares whether or not the data is valid. If valid, the appropriate "1" or "0" line to the encrypter is activated, and if not valid, the "S" line is activated. The data bits are then sent to the encrypter via differential drivers and upon the next modulator interrupt a clock pulse (gated by the clock enable) is sent to the encrypter. The same clock signal is used to strobe the contents of the encrypter output into the output registers. Concurrently, the buffer registers are also updated. Between Modulator interrupts, the clock is inhibited by the logic zero value of the clock enable signal.

Reading the contents of the output register consists of issuing a load instruction from memory location 176041. The address interface logic enables the contents of the output buffer register onto the μ P local data bus and generates an ACKN- signal.

Figure 3-6 is a timing diagram for the Encrypter Interface logic.

External Signal Interface

The external signal interface consists of seven twisted pair wires (3 data in, 3 data out, and one clock, all enclosed in an overall shield. Differential line drivers and receivers are utilized.

3.4 Voice Interface and Encrypter Interface Addressing

Address decode logic is common to both interface units. The decode logic is activated when the upper 13 address bits are 17604X and performs a further decode on the lower 3 bits to enable the appropriate control signals. A CBACK- signal is generated in response to a correctly addressed Load or Store signal. Table 3-1 lists the functions generated by each address decode. Locations 176045 & 176046 are unique to the Voice Interface, while 176040 & 176041 address only the Encrypter interface. The program clear (location 176047) is common to both functions.

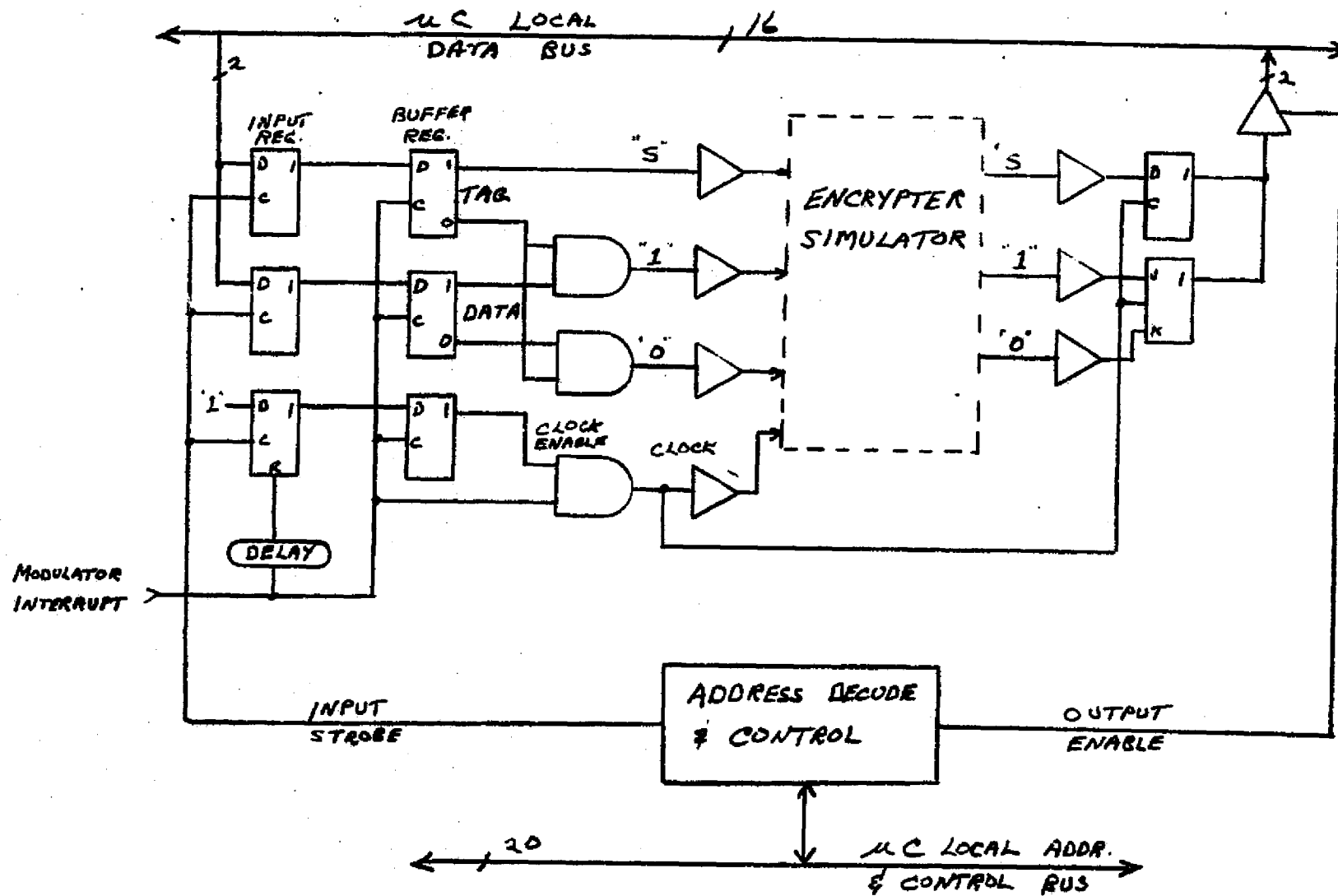


FIG 3-5

ENCRIPTOR INTERFACE DETAILED BLOCK DIAG.

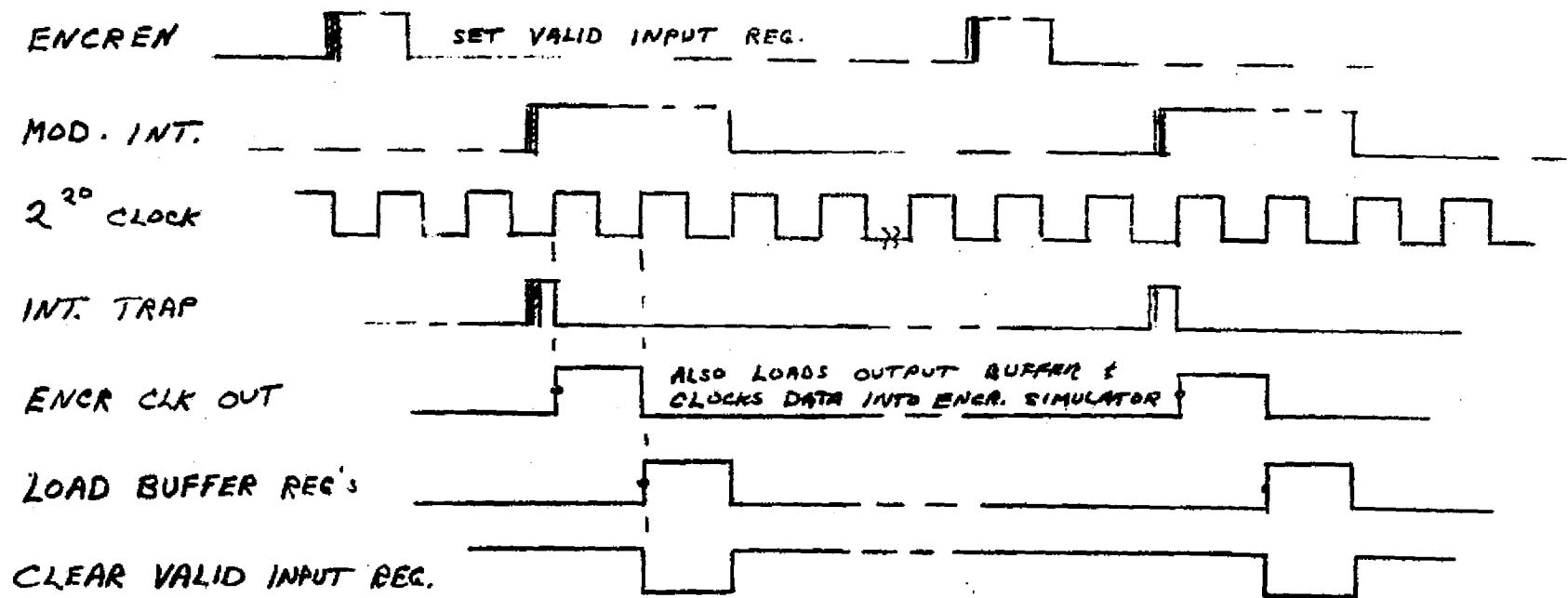


FIG. 3-6
ENCRYPTOR INTERFACE TIMING.

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Address	Function	Data Bits		
		CBD15,	CBD14	-----
176040	Load Encrypter Interface Input Registers.	Tag bit	Data Bit	
176041	Read Encrypter Output Registers			
176042	Not Used			
176043	" "			
176044	" "			
176045	Voice Interface Test Mode			
176046	Read Voice Interface Output Register	First Input Bit	-----	-----
176047	Program Clear			

Table 3-1

3.5 Detailed Logic Schematic

The detailed logic design for the Voice and Encrypter Interface logic is shown on the two logic drawings listed below:

DWG. No.	Sheet #	Logic
893202	1	Voice Interface
	2	Encrypter Interface

4.0 COMMAND ENCODER BCH ENCODER MODULE

The BCH Encoder is required for expansion of a 48-bit data word into a 128-bit word comprised of a) three zeros or dummy bits, b) the original 48 bits, and c) 77 special parity check bits.

4.1 General Description

A functional block diagram of the BCH Encoder is shown in figure 4-1. The hardware consists of a 50 bit shift register, BCH encoding logic and appropriate timing control. Its operation basically entails:

- a. outputting the 48 data bits from the Microcontroller to the shift register via three 16-bit word transfers

4.1 (General Description, Continued)

- b. inputting the first 16-bit word from the shift register to the microprocessor with the 3 MSB's set to "0".
- c. issuing a "go" command to the control logic
- d. waiting for an interrupt to indicate when the next 16 output bits have been accumulated in the shift register
- e. inputting the 16 bits of the shift register into the Microprocessor (Note: interrupt response time is not critical since the hardware automatically shuts itself down after each 16 bits).
- f. repeating steps b) - d) six more times

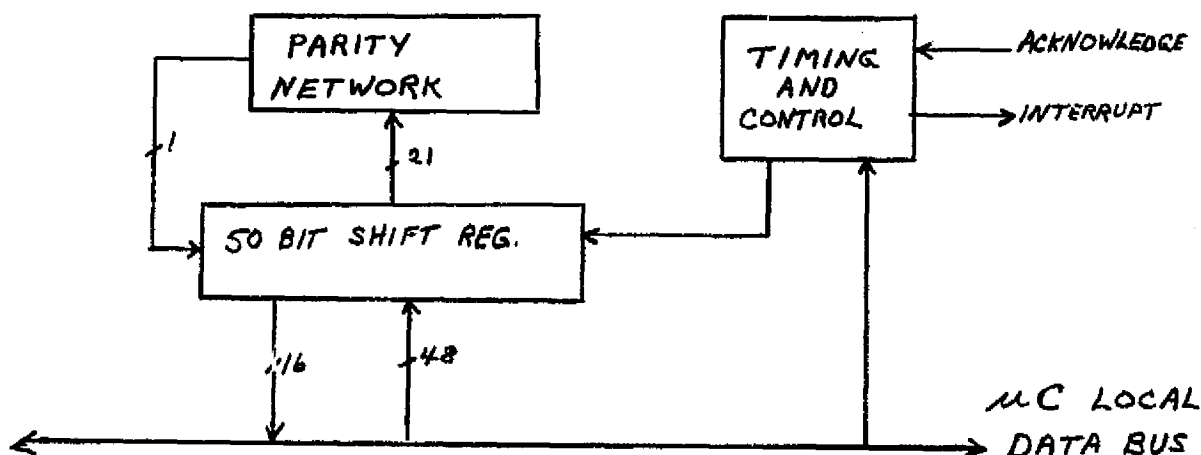


Figure 4-1 BCH Encoder Functional Block Diagram

4.2 Functional Description

The detailed block diagram of figure 4-2 identifies the component areas which are discussed in the following sections.

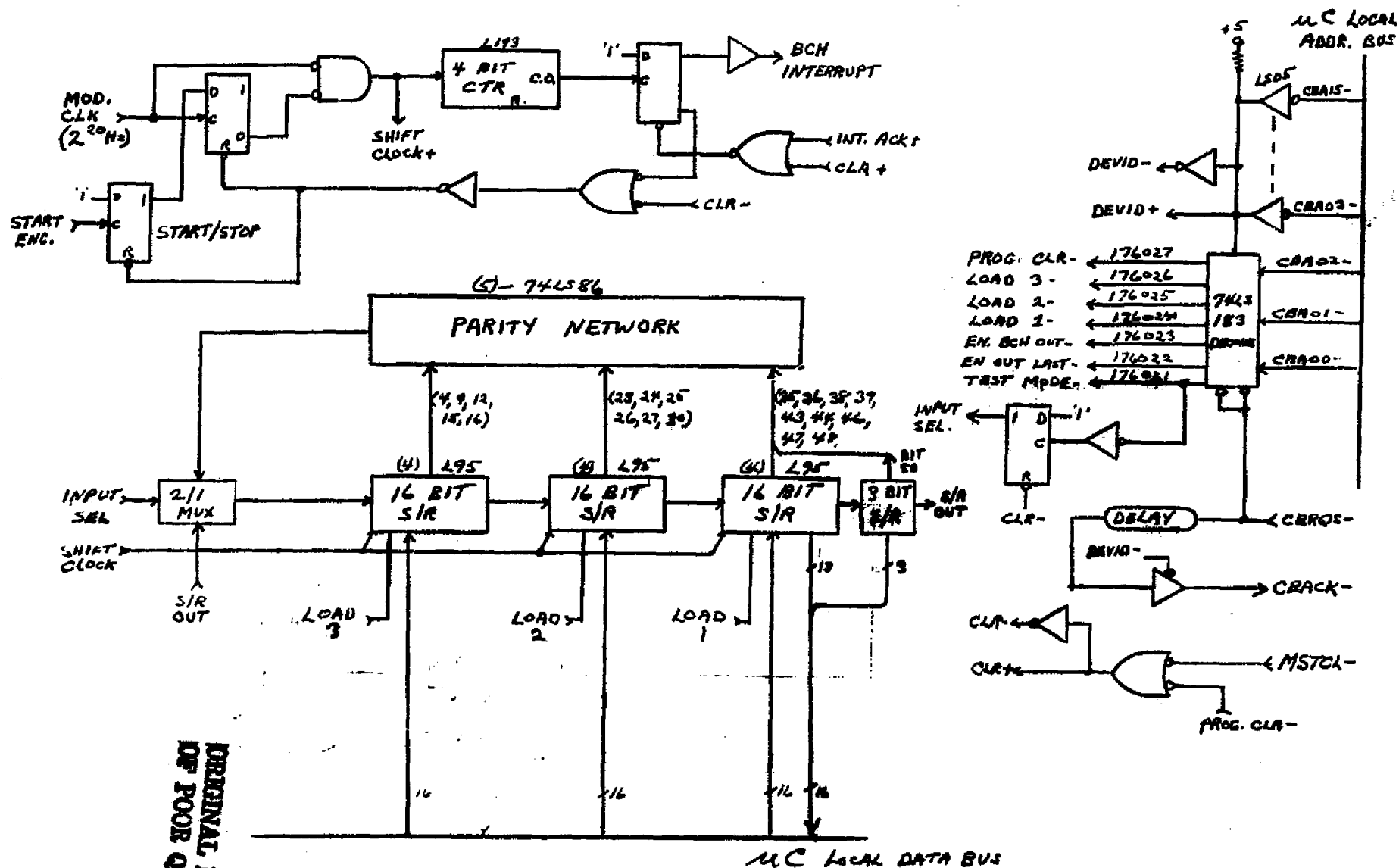
4.2.1 Encoder Load Sequence

Three microprocessor (μP) store instructions (to memory locations 176024, 176025 and 176026) are issued to load bit 0 to 48 of the dual function input shift register with the non-encoded command word. Bits 49, 50 and 51 are cleared to zero by the shift register load clock.

The three dedicated register load signals are generated by decoding the μP local address during each store operation.

4.2.2 Encoding

The encoding operation is initiated following the third load command which sets the start/stop flop, enabling the 2²⁰ Hz modulator clock into the BCH encoder.



4.2.2 (Encoding, Continued)

During each clock period, the BCH encoding logic calculates even parity on bits 4,9,12,15,16,23,24,25,26,27,30,35,36,38,39,43,44,46,47,48 and 50 of the shift register. Simultaneously a 4-bit counter is incremented to keep track of the number of encoder shift pulses.

4.2.3 Encoder Output Sequence

The sixteenth clock pulse causes the 4-bit counter to overflow (carry-out) and set the BCH interrupt flop, which in turn resets the start/stop flop. The BCH interrupt flop is reset by the automatically generated BCH Interrupt Acknowledge signal from the Priority Interrupt Network. The content of the shift register, bits 36 through 51 is read onto the μP data bus by issuing a load instruction from memory location 176023.

The BCH Encoder is restarted by the trailing edge of the load Acknowledge signal and four more encoding cycles must be executed to accumulate the resultant 80 bits (16 x 5).

4.2.4 Encoder Addressing

The address interface logic is activated when the upper 13 address bits are 17602X and performs a further decode on the lower 3 bits to enable the appropriate control signals. A CBACK- signal is generated in response to a correctly addressed Load or Store signal. Table 4-1 lists the functions generated by each address decode.

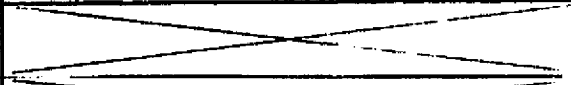
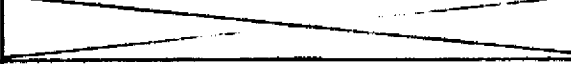
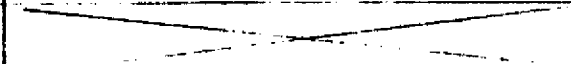
Address	FUNCTION	DATA BITS
		CBD15 - - - - - CBD0
176020	Not Used	
176021	Encoder Test Mode	
176022	Read Last (5th) Encoder Word	MSB - - - - - LSB
176023	Read Encoder Words 1-4	MSB - - - - - LSB
176024	Load Word 1 (bits 1-16 of command message)	MSB - - - - - LSB
176025	Load Word 2 (Bits 17-32 of command message)	MSB - - - - - LSB
176026	Load Word 3 (Bits 32-48 of command message)	MSB - - - - - LSB
176027	Encoder Programmable Clear	

Table 4-1 BCH Encoder Address Decode Functions

4.2.5 Bus Interface & Control

The data bus interface is tri-state, operating at standard 54/74 series TTL voltage levels. Bus drivers are held in the high impedance state until a μ P fetch operation from locations 176022 or 176023 is issued and decoded. Drivers are National tri-state inverting buffers, DM8098.

Bus activity is controlled by a Request (CBRQS-) signal from the μ P and an Acknowledgement (BCHACK-) signal returned from the BCH Encoder. The Request line initiates a bus cycle, while the Acknowledgement line signifies the completion of the Encoder response: For a load operation, the transition of the Request line from high to low indicates a valid address and data. The transition of the BCH Encoder Acknowledgement from high to low indicates that the data has been accepted.

For a read operation, the transition of the Request line again indicates a valid address. The transition of the Acknowledgement signal from high to low signifies that valid data is available to the μ P.

4.3 Encoder Timing

Figure 4-3 illustrates the BCH Encoder signal timing which is referenced to the modulator clock, and the μ P CBRQS signal.

4.4 Encoder Sequence Flow-Chart

A flow chart of the Encoder sequence of operation is shown in Figure 4-4.

4.5 Built-In Test Equipment (BITE)

An encoder test mode is available for aid in debug and fault isolation. When selected, the test mode allows the 50-bit shift register to operate in a closed loop mode, with bit 51 fed into bit 1. Data can then be loaded into the shift register, cycled through the normal 16-bit shift sequences, and then read out. The parity logic output is removed from the register input in the test mode. The Encoder remains in the test mode until a clear signal is issued.

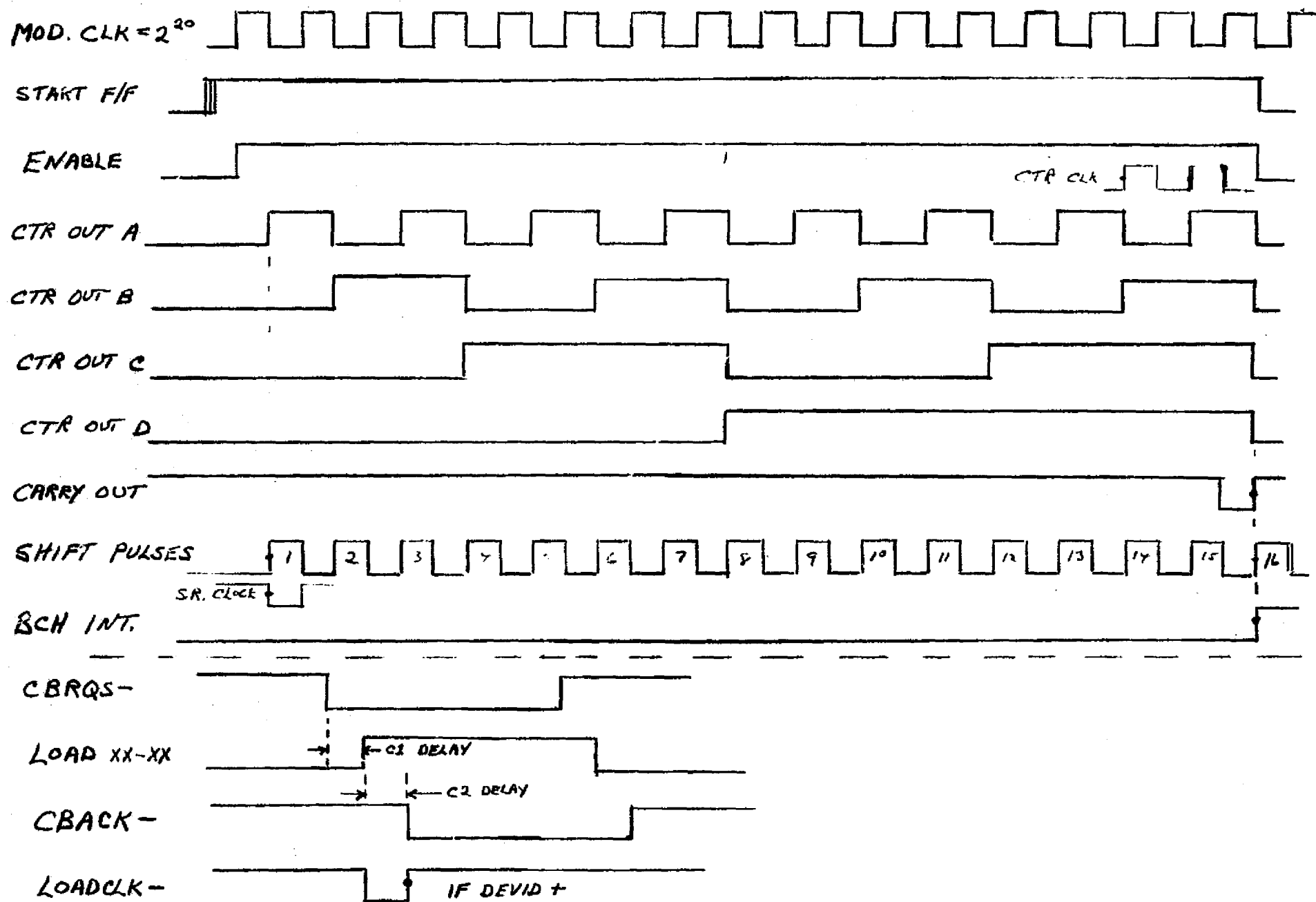
4.6 BCH Encoder Clear Signal Generation

The Encoder can be cleared by either of two signals: a program generated clear (address 176027) or by a μ P bus signal master clear (MSTCL-).

4.7 Detailed Logic Schematics

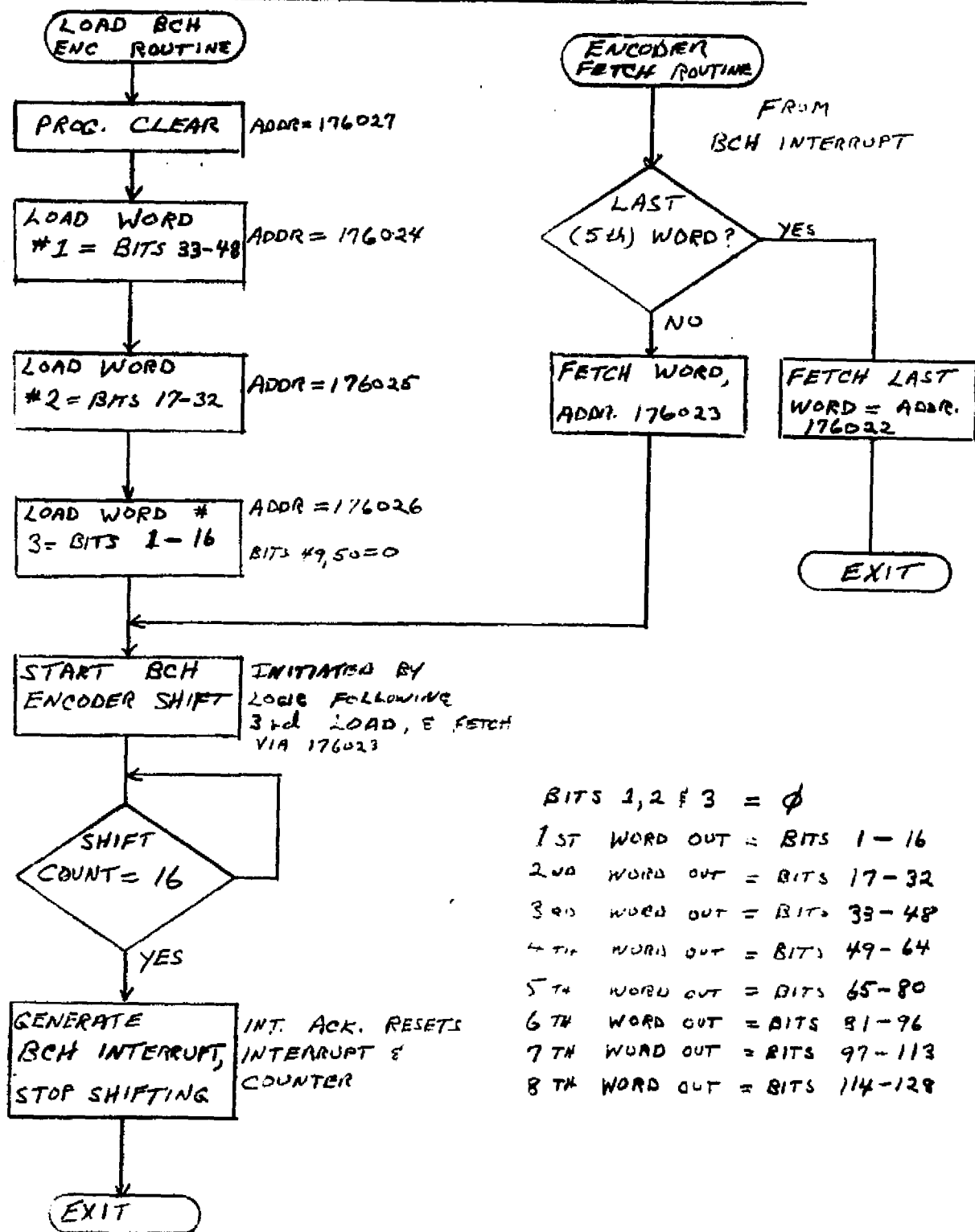
The detailed logic design for the BCH Encoder is shown in the two logic diagrams listed below:

DWG. No.	SHEET #	Logic
893201	1	shift register, parity logic, bus drivers and input buffers
	2	Control Logic, address decode logic



BCH ENCODER TIMING. Fig. 4-3

BCH ENCODER FLOWCHART



BITS 1, 2 & 3 = ϕ

- 1ST WORD OUT = BITS 1-16
- 2ND WORD OUT = BITS 17-32
- 3RD WORD OUT = BITS 33-48
- 4TH WORD OUT = BITS 49-64
- 5TH WORD OUT = BITS 65-80
- 6TH WORD OUT = BITS 81-96
- 7TH WORD OUT = BITS 97-113
- 8TH WORD OUT = BITS 114-128

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FIG. 4-4

5.0 MICROPROCESSOR

The Microprocessor (μ P) is an existing Raytheon (RP-16) device designed specifically for data processing and control application of the type under consideration here. It consists of an arithmetic unit, a control unit, and bus interfaces. These are described briefly in the following paragraphs.

5.1 Arithmetic Unit

The Arithmetic Unit (AU), shown in Figure 5-1, is divided into six parts: Data Multiplexers, Register File, Arithmetic Logic Unit (ALU), Status Generator, Data Drivers and Address Drivers. Multiple use is made of as much hardware as possible. A single register file contains all program-accessible data, a Working Register (WR) and an Address Register (AR). The WR is used both as a data bus input register and as a holding register for intermediate results in certain algorithms. The AR serves as a shift counter and an iteration counter as well as a calculated address register. The Arithmetic Logic Unit performs all data and address manipulation and a single multiplexer array, which precedes the file input, performs all data source selection and end condition specification.

5.2 Control Unit

The Control Unit is microprogrammed. Each micro-instruction is made up of one or more primitive micro-operations which are executed in parallel during the clock-pulse-to-clock-pulse time frame of the micro-instruction. During the clock interval, the logic process is entirely combinational. When the clock period ends, all storage elements are updated and another sequential step in the process is completed.

The μ P control unit (Figure 5-2) divides into several parts: the sequence and control function previously described, and a number of subordinate functions, none of which require more than a half dozen or so ICs to implement.

5.3 Bus Interfaces

The μ P bus contains 16 lines of data, 16 lines of address and 4 lines of control. A Request control line activated either by the μ P or by an external source initiates a data transfer cycle to or from a memory or I/O device that recognizes its address on the address bus. The proper address must be on the bus for the duration of a valid Request signal. Also, if data is being stored to memory or I/O, this information must be placed on the data bus for the duration of Request. Fetch or Store mode is specified by a Write control line sent from the μ P or external source. This signal must also be established for the duration of a valid Request signal.

A memory responds to the Request Line with an Acknowledge signal when a memory cycle is completed. For a store, Acknowledge occurs when data has been written into the addressed memory location from the data bus. For a fetch, Acknowledge occurs when the contents of the addressed memory location have been placed on the data bus. This data remains on the bus until Request terminates.

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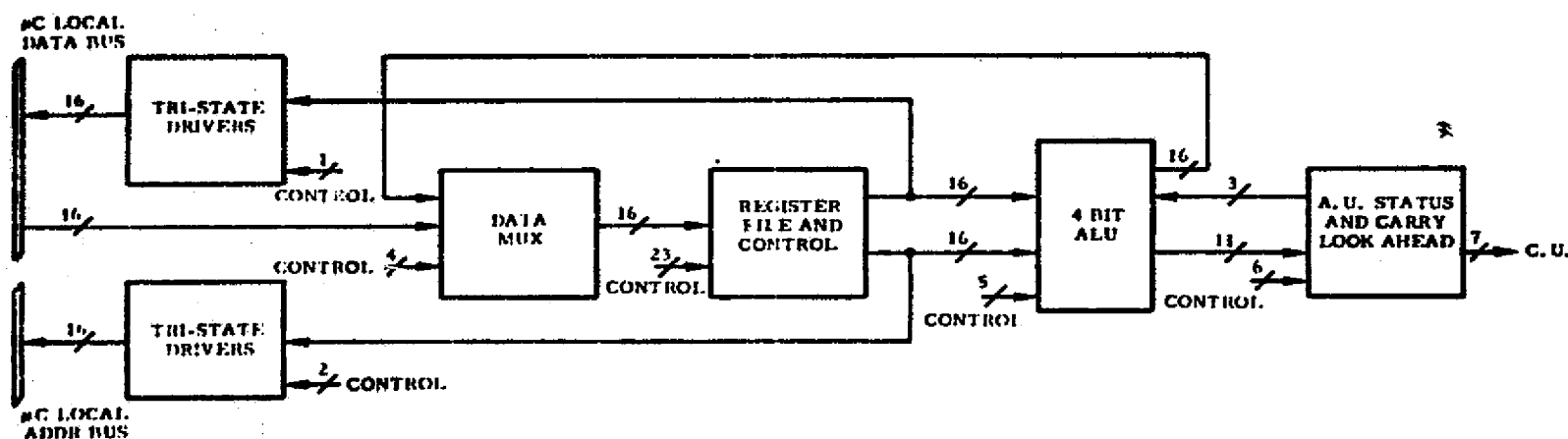


Figure 5 -1 Arithmetic Unit Block Diagram

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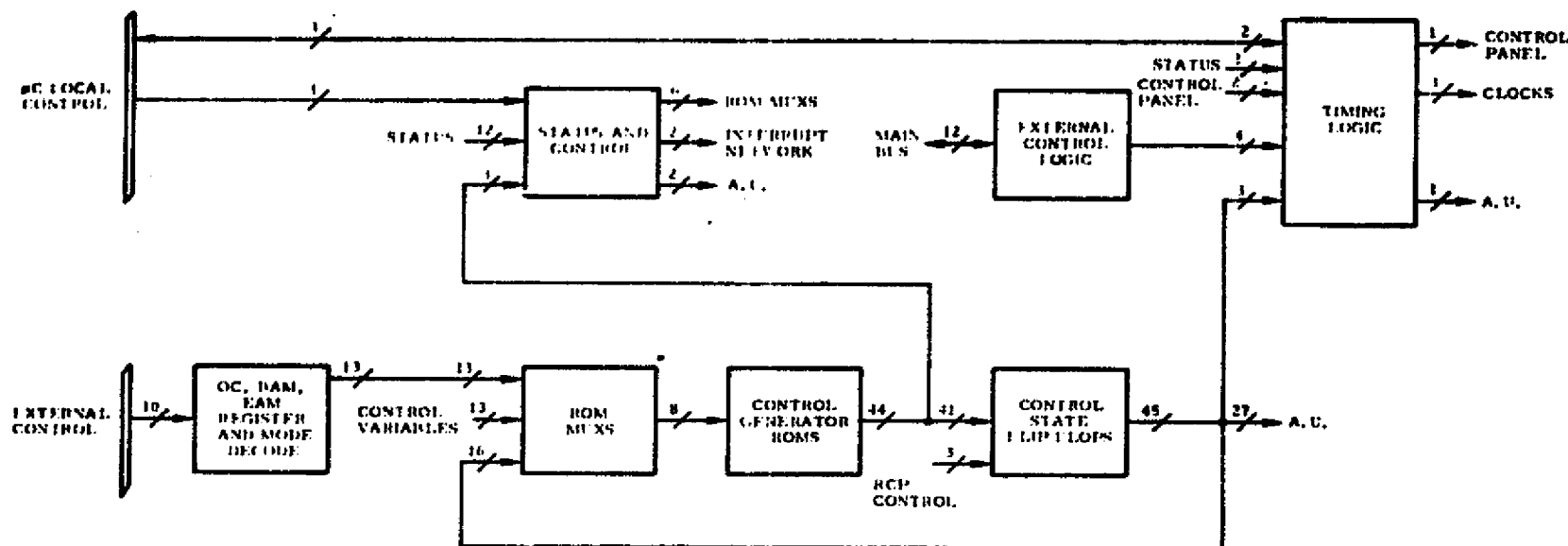


Figure 5-2 Control Unit Block Diagram

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5.3 (Bus Interfaces, Continued)

An acknowledge signal for a fetch cycle received either by the μP or by an external source causes data on the data bus to be loaded into an internal register. For a fetch or store cycle, an active Acknowledge signal causes termination of the source Request line. Termination of Request in turn causes memory to remove Acknowledge, completing a totally asynchronous transfer cycle.

Asynchronous data transfers are performed with I/O devices in the same manner, with one exception. An optional fourth control line, called the Skip signal, is used to notify the source of the status of the data transfer, and must be valid for the duration of the peripheral Acknowledge. An activated Skip line will cause the Microcontroller to skip over its next program instruction. The Skip line can be activated by a peripheral for either the transfer or no transfer condition, depending upon designer's choice.

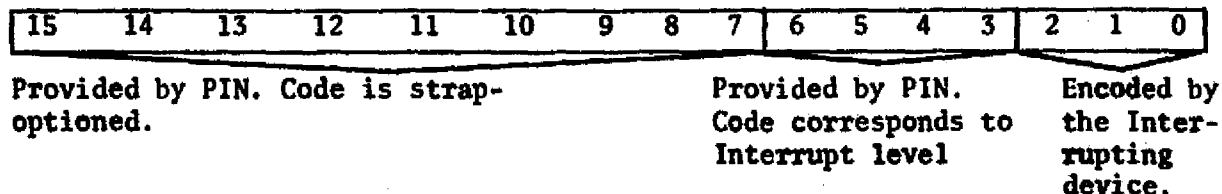
5.4 Priority Interrupt Network

Sixteen interrupt levels are provided in the μP through the use of a Priority Interrupt Network (PIN) module. As can be seen in Figure 5-3, this module contains the following:

- A 16-bit latch, up-dated at the end of each instruction fetch
- A 16-line priority encoder which produces a 4-bit code corresponding to the highest level present in the latch.
- A 4-bit "Allowed level" latch, which in conjunction with a 4-bit comparator determines if the highest interrupt present equals or exceeds the allowed level determined by software. The 4-bit latch is accessible in the same way as any other I/O device, and can be written into or read from at any time.
- A 4-bit-to-16-line decoder which issues an acknowledge level corresponding to the level of interrupt being serviced.
- Miscellaneous control logic, address drivers, etc.

Operation of the PIN is as follows:

- Interrupt priority is established
- Encoded level is compared with current allowed level
- If allowed, an Interrupt Request is issued to the μP
- Upon acknowledge from the μP , ACK(n) is issued to interrupting device
- Concurrently with (d), the μP is prevented from putting address 0 or 1 on the bus. Instead, the PIN places address bits 3 through 15 on the bus, while the interrupting device provides address bits 0, 1, and 2 as shown in the following diagram:



- The trap location to be loaded into P is obtained from memory at the address defined by the above scheme.

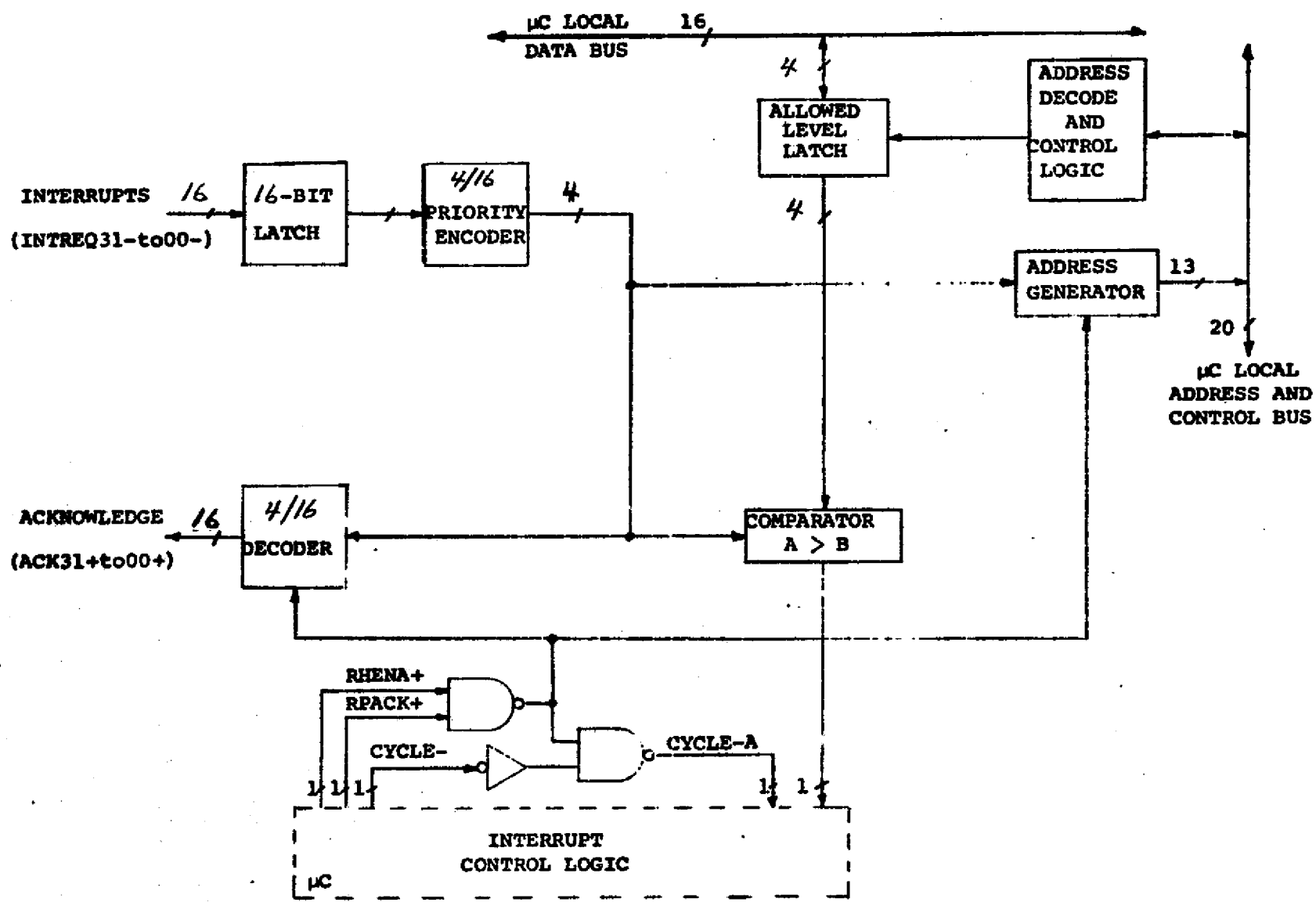


Figure 5 -3 Priority Interrupt Network Block Diagram

2-115

5.4 (Priority Interrupt Network, Continued)

In this fashion, each of the two built-in levels of interrupt is expanded to 16 levels, with a corresponding 128-word trap table held in memory. As system software dictates, the trap table can be modified dynamically, as can the allowed level of interrupt (individual level masks are located on the devices themselves).

5.5 CE Random Access Memory (RAM)

Two modules are required to implement the 5120 word X 16 bit CE memory. One is a 1024 word X 16 bit bipolar two-port memory with interrupt capability, and the second is a 4096 word X 16 bit MOS two-port memory. Each module has self-contained logic to interface with two independent (external master and local micro-processor) ports. Data is provided on two 16 bit bilateral data busses and the address information is provided on a 16 bit unilateral bus. Each port interface uses two interface "handshaking" lines (Request and Acknowledge) and one mode line (Read/Write). Also provided on the bipolar memory, are two interrupt flops which are set when the external port writes into a specified address and reset when the μ P port reads that location. A port selects the RAM by correctly addressing the port discriminator (with the upper six address bits) prior to generating its request signal. If this port wins, the port discriminator effectively connects the memory to the appropriate port (by steering the data, address and mode multiplexers), and it receives a positive response from the RAM timing logic on its acknowledge line. Once a port is selected, the RAM is busy until the requesting port removes its request line, which in turn allows the RAM to service other requests. Port selection is on a first come, first serve basis with internal hysteresis resolving simultaneous requests. Note that the losing interface will receive service within one memory cycle - 1000 ns. Conflicts cannot occur more than once per 30us (data bus rate) and hence are insignificant.

5.5.1 CE Memory Map

Figure 5-4 is a memory map of the CE octal address spectrum. Addresses 0 to 1777 are located in the 1024 word, RAM, addresses 10000 to 17777 are located in the 4096 word RAM, while addresses 176000 to 17776 are reserved for hardware registers by the local data bus. Each register is accessed as a unique address in the overall address spectrum.

5.5.2 CE Interrupt Trap Addresses

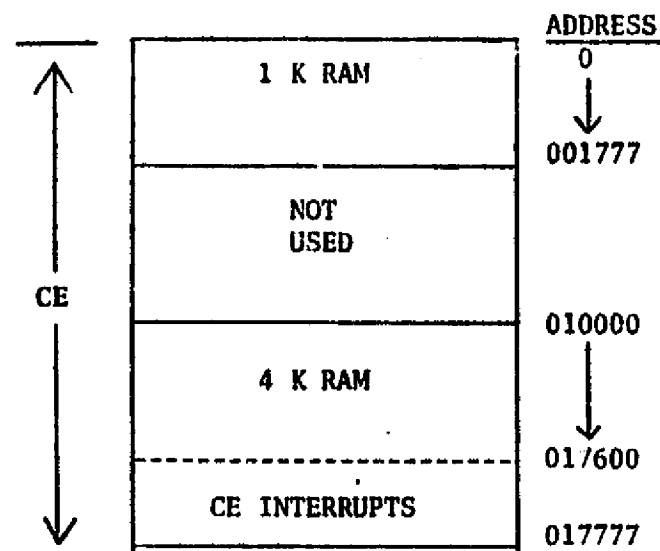
The CE interrupt trap addresses are listed below in order of ascending priority.

INTERRUPTS:

TTY	017610	Level 1
Tape Reader	017620	" 2
C. Ch. Mess.	017630	" 3
PMS Ch. Mess.	017640	" 4
BCH Encoder	017670	" 7
Interval Timer	017700	" 8
Voice Int.	017720	" 10
Mod. Data S. Req.	017740	" 12
Mod. Act. Det.	017741	" 12
Hung Bus Det.	017770	" 15

CE MEMORY MAP

Figure 5-4



PERIPHERAL ADDRESSES:

ALCM *	176000
BCH Encoder	176020
Encrypter Inter.	176040-41
Voice Interface	176045-47
Pin Mask	177376
Boot Strap *	177400
Modulator	176100

* NOT USED

C. CE TEST SET HARDWARE

The following sections define the operation of the CE Test Set functional units.

1.0 CE TEST SET MICROPROCESSOR

The CE Test Set incorporates an RP-16 microprocessor identical to that described in section B, 5.0 for the CE. Associated peripheral and memory modules required for the CE Test Set are described in the following sections.

1.1 Peripheral Modules

Three additional peripheral modules are required in the CE Test Set; an asynchronous line control module (ALCM), a perforated tape reader/punch interface module, and a local control panel (LCP) interface module. The following sections briefly describe the functional operation of each module and the LCP. Detailed operational characteristics are contained in the functional specification for each module.

1.1.1 ALCM Module

Purpose

The ALCM is a single 6" x 8" two-sided PCB designed to fulfill virtually all serial asynchronous communications applications for systems employing the Raytheon RP-16 microprocessor. It interfaces directly to the microprocessor I/O bus, and has on-card circuitry for sending and receiving 20 ma loop signals to/from a TTY. In addition, the capability to interface to a Modem (e.g., 103 A2, 202 C6, etc.) is present including the EIA RS-232C/MIL-STD-188C drivers and receivers.

I/O Interface Specifications

Communications Mode:	Full or Half-Duplex, or Simplex
Format:	Serial, asynchronous
Bit Rates:	110, 150, 300, 600, 1200, 2400, 4800, 9600 Baud on-card (external clock [XMIT and RCV] pins are available)
Character Length:	5, 6, 7, or 8 bits
Parity:	Even, odd, or none
Stop Bits:	1 or 2 (1-1/2 available on 5-bit char length)
Levels:	20 ma loop, TTL, for XMT and RCV Data, all signals EIA RS-232C or MIL-STD-188C

1.1.2 Perforated Tape Reader/Punch Interface Module

Reader Interface

The Perforated Tape Reader portion of the Interface possesses the following functional characteristics:

- a) Able to handle data fields up to 8-bits wide

(Reader Interface, Continued)

- b) Bidirectional control of tape movement
- c) Able to operate in either the interrupt mode or under sole control of the "skip" line.
- d) Able to report up to two status bits of which one will cause a program interrupt to the RP-16 providing interrupts are unmasked and enabled.
- e) Single character buffering of the data

Punch Interface

The perforated Tape Punch portion of the Interface possesses the following functional characteristics:

- a) Able to perforate tape with data fields up to 8 bits wide
- b) Able to operate in either the interrupt mode or under the sole control of the "skip" line.
- c) Able to report up to four bits of punch status of which three will cause a RP-16 program interrupt if interrupts are unmasked and enabled.
- d) Single character buffering of the data.

1.1.3 Local Control Panel

The Local Control Panel (LCP) is a front mounted, 19-inch rack panel which contains the necessary switches, displays, and logic to manually control a μ P. One LCP is provided with the CE system and will normally be mounted in the test set and connected to the test set μ P. It could, however, be removed from the test set and connected to the CE μ P for troubleshooting, if desired. Interface from the LCP to the μ P is through four ribbon cables to an adapter card which plugs into the card cage adjacent to the CPU modules.

Panel Layout

Figure 1-1 shows a sketch of the front panel layout for the LCP. A bank of 16 lights (LED's) is provided to display selected data, while a bank of 16 toggle switches allows the operator to enter new data. Two rotary switches provide for Register Select and Mode Select. There is an Execute pushbutton, as well as a Power On light and a Run light.

Block Diagram

Figure 1-2 shows a block diagram of the LCP logic and its interface to the μ P. The logic is contained on a PC board, which is mounted directly behind the LCP front panel. Lights and switches are directly mounted on the same PC board, minimizing assembly and inter-wiring time.

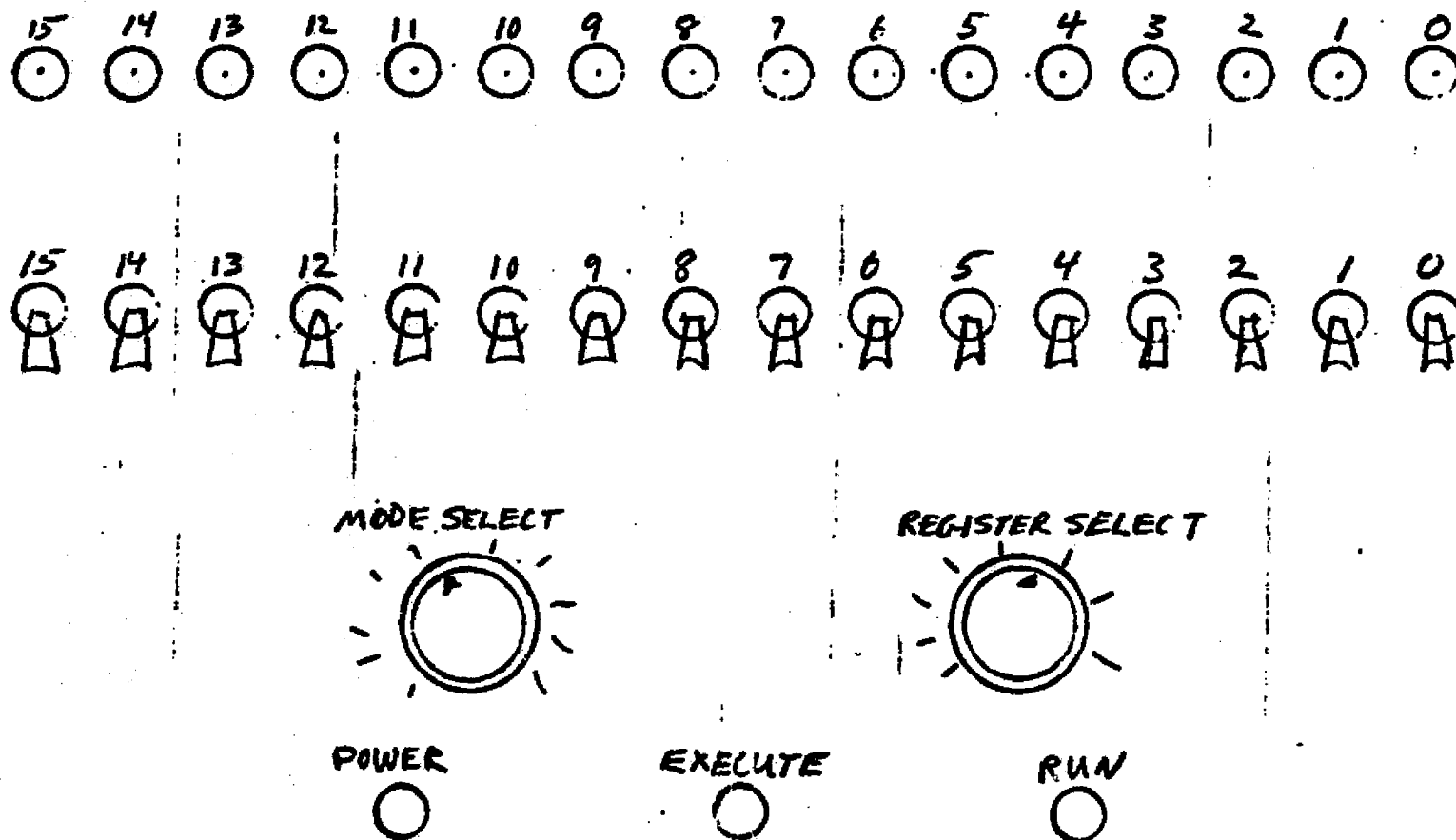
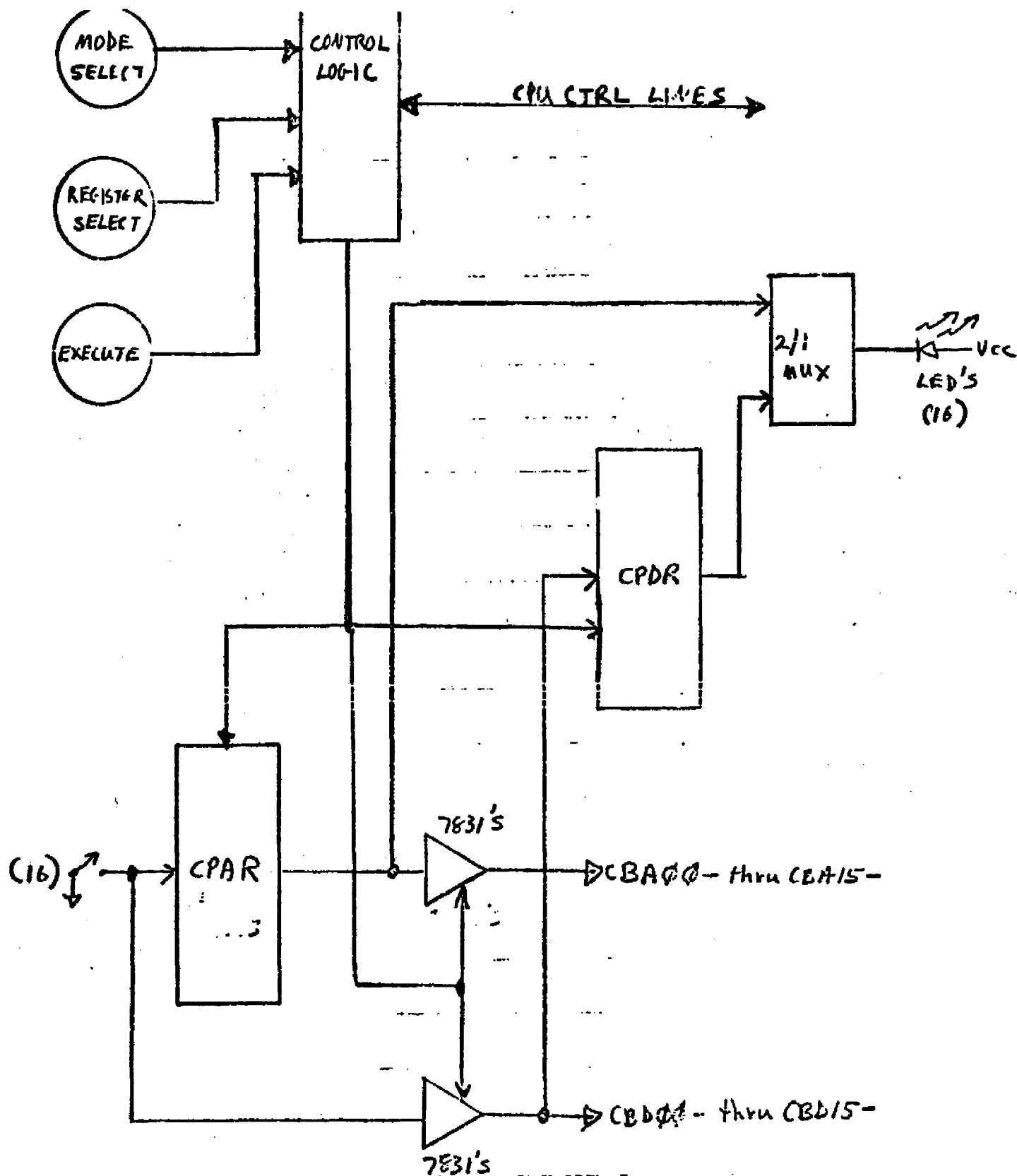


FIGURE 1-1

LCP LAYOUT SKETCH (NOT TO SCALE)



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FIGURE 1-2

LCP BLOCK DIAGRAM

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Operation

The following table enumerates the actions taken by the LCP, dependent on operator switch settings. In all cases, any of the data switches in the up position signifies a "logic 1", while the DOWN position indicates a "logic 0", for the corresponding bit position. The data lights and switches are arranged with MSB to the left.

LCP OPERATIONS TABLE

MODE SELECT ROTARY SWITCH	REGISTER SELECT ROTARY SWITCH	EXECUTE ACTION
STORE 1	N/A	Store contents of data switches in memory location specified by Control Panel Address Register (CPAR). Increment CPAR at end of cycle. Contents of new address are fetched and displayed.
FETCH 1	N/A	Read contents of memory location specified by CPAR. Deposit in Control Panel Data Register (CPDR). Post-Increment CPAR. Data switches have no effect.
STORE	N/A	Same as STORE 1, except CPAR is <u>not</u> post-incremented. New contents of memory are fetched and displayed.
FETCH	N/A	Same as FETCH 1, except CPAR is <u>not</u> post-incremented.
ADDRESS SELECT	N/A	Store contents of Data Switches in CPAR. CPAR is displayed in Data Lights.
REGISTER SELECT	S	Store contents of switches in S. S displayed.
	P	Store contents of switches in P. P displayed.
	B	Store contents of switches in B. B displayed.
	X	Store contents of switches in X. X displayed.
	A	Store contents of switches in A. A displayed.
	E	Store contents of switches in E. E displayed.

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MODE SELECT ROTARY SWITCH	REGISTER SELECT ROTARY SWITCH	EXECUTE ACTION
REGISTER SELECT (continued)	WR	Store contents of switches in WR. WR displayed.
	AR	Store contents of switches in AR. AR displayed.
HALT	N/A	A 2-word instruction is sent to the Control Register of the CPU. The CPU is halted. Current contents of selected register are displayed.
RUN	N/A	A 2-word instruction is sent to the Control Register of the CPU. The CPU assumes the RUN state. CPU data bus is monitored in the Display Lights.
INR STEP	N/A	A 2-word instruction is sent to the Control Register of the CPU. The CPU assumes the RUN state for one(1) program instruction, then halts. Current contents of selected register are displayed.
MASTER CLEAR	N/A	MSICL signal sent to CPU. Current contents of selected register are displayed.

1.2 CE Test Set Random Access Memory (RAM)

Two memory modules provide the 6144 words of 16 bit RAM for the Test Set Microprocessor. One module is a single port 2048 word by 16 bit MOS memory and the other is a dual port 4096 word by 16 bit MOS memory, using one port only. The memory I/O ports are connected to the test set local data bus which interfaces with the CE RAM external master port.

1.3 Test Set Memory Map

Figure 1-3 is a memory map of the combined CE and test set octal address spectrum. Test set memory addresses are contiguous from location 20000 through 33777.

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MEMORY MAP

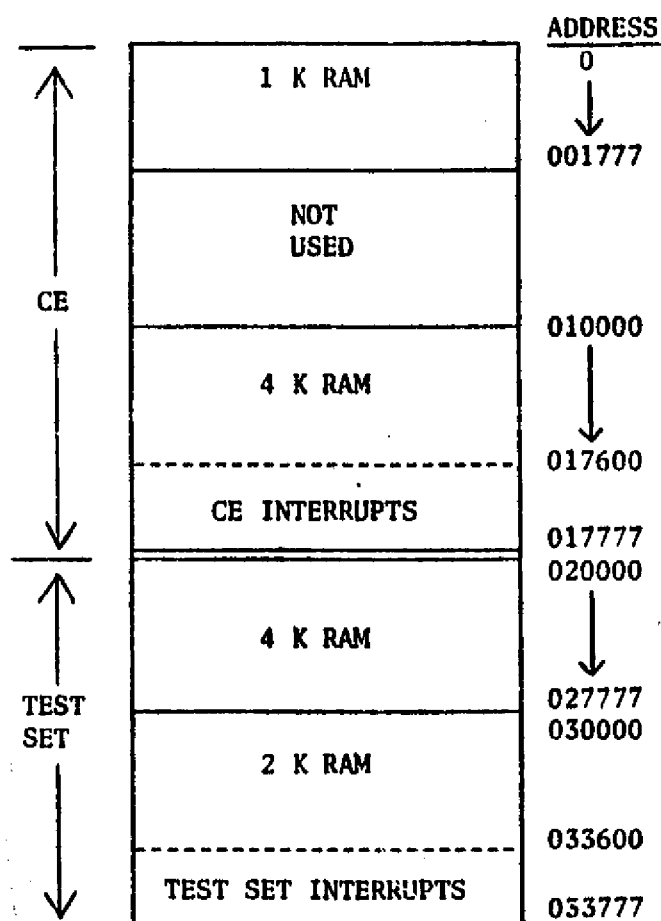


FIGURE 1-3

1.3 Test Set Memory Map (Continued)

Test Set Interrupt Trap Addresses

The test set interrupt trap addresses are listed below in order of ascending priority.

INTERRUPTS

TTY	033610	Level 1
Tape Reader	033620	" 2
BCH Encoder	033670	" 7
Demodulator	033740	" 12
* CE Error Int.	033750	" 13
Hung Bus Det.	033770	" 15

* Not Connected

Peripheral Addresses

Addresses 176000 to 17776 are reserved for hardware registers on the local data bus. Each register is accessed as a unique address in the overall address spectrum.

PERIPHERAL ADDRESSES

ALCM	176000
BCH Encoder	176020
Tape Reader	176120
Demodulator	176140
Encryptor Simulator	176160
Voice Simulator	176164
Pin Mask	177376
Boot Strap	177400

2.0 CE TEST SET BCH ENCODER

The test set BCH encoder module is a duplicate of the encoder module used in the CE. Refer to section B, 4.0 for functional details.

3.0 COMMAND ENCODER TEST SET DEMODULATOR

The Demodulator portion of the Test Set serves to decode the data contained in each of the seven (7) types of crosslink signals for transmission to the microprocessor to be evaluated. Depending on the transmission mode, data is either accumulated into words or sent bit-by-bit onto a common 16 bit data bus. An overview of the Test Set Demodulator showing its interfaces is shown in Figure 3-1.

3.1 Functional Description

The Demodulator Block Diagram in Figure 3-2 shows the functional blocks comprising the overall demodulator. The Analog Mux buffers all transmissions received on the crosslink line and sorts the conditioned signal to one of six bit/word clock and data detectors. The demodulated data from the detector in use is then loaded into a buffer for retrieval by the microprocessor.

The microprocessor is a natural for performing the comparison between intended data and that detected from the crosslink. However, it became necessary to compromise the bit-by-bit error detection because of high data rates in some modes. As a result, the word clock may load data in 1, 5 or 16 bit words onto the bus depending on the mode of operation.

Although each transmission mode is unique, there are similarities that allow sharing of common hardware since only one mode is active at a time. Those functions that utilize common hardware are as follows.

②

TO MICROPROCESSOR
& OTHER PERIPHERALS

CONTROL BUS ADDRESS BUS DATA BUS

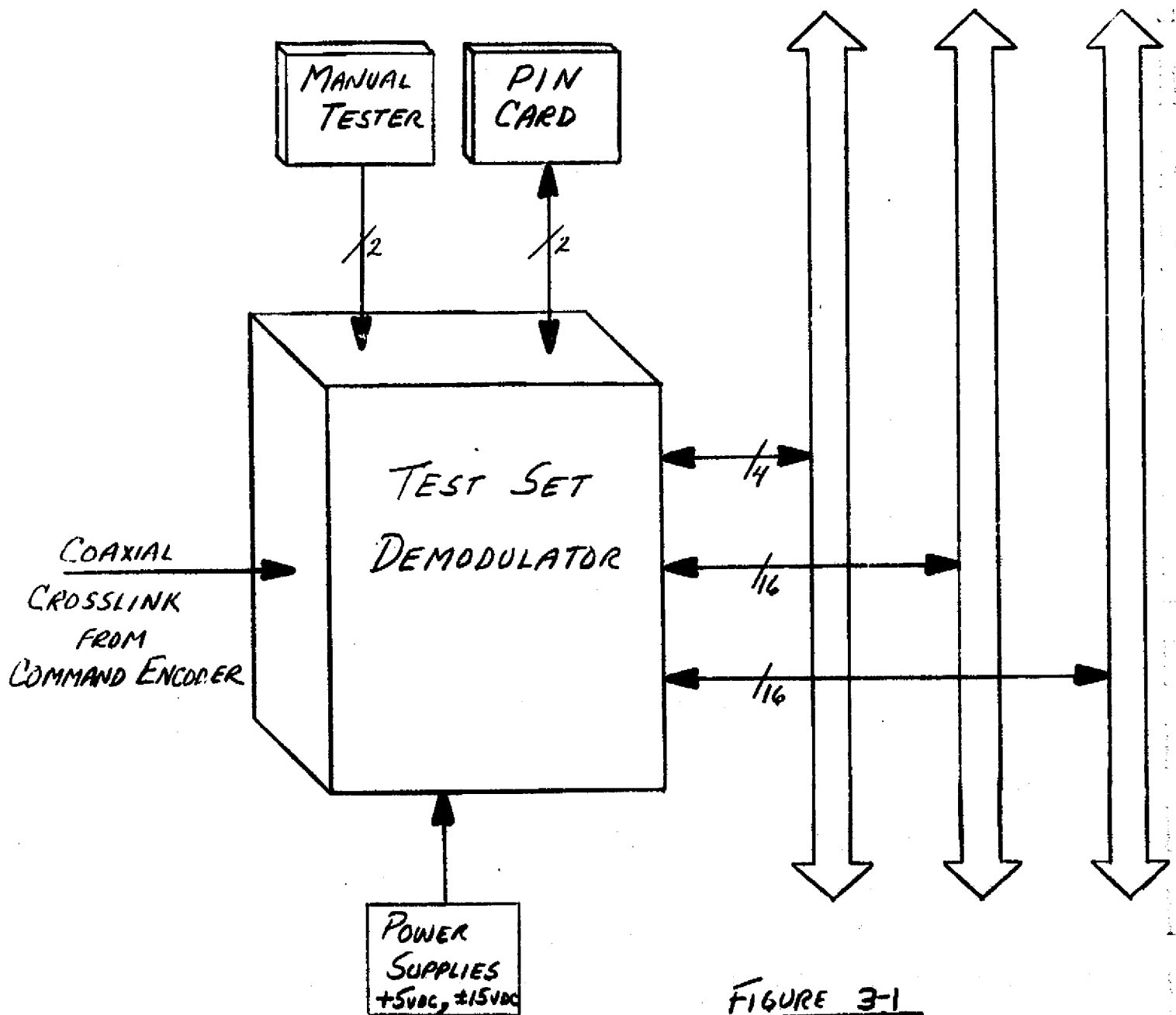


FIGURE 3-1

REV NO.	DR <i>Tom Wright</i>	DATE <i>5 May '75</i>	CLASSN <i>CM</i>
REVISIONS	TEST SET DEMODULATOR I/O		
	RAYTHEON	A	SK-REWS MAY '75-1
			REV 9

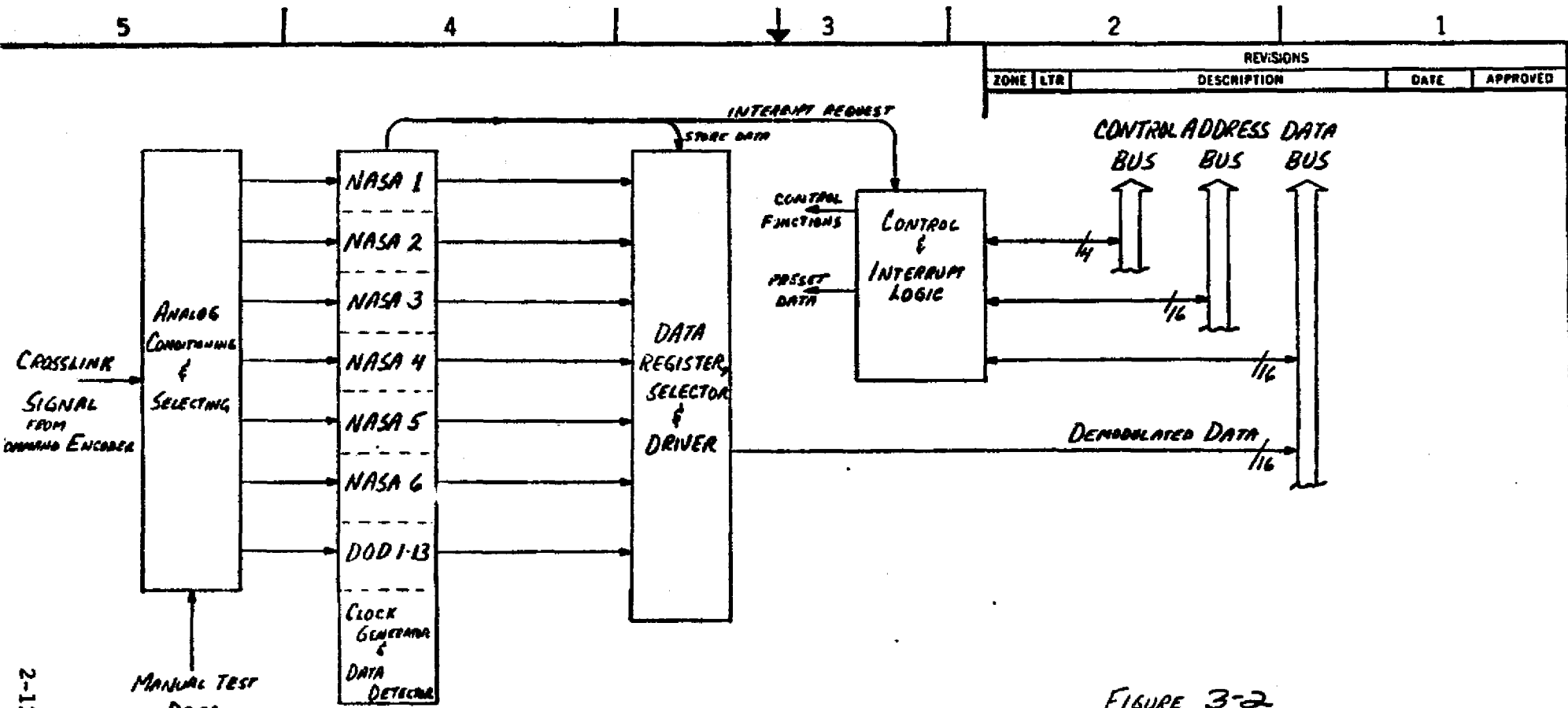


FIGURE 3-2

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QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.
PARTS LIST					
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR. NO.	<div style="display: flex; align-items: center;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">RAYTHEON</div> <div>RAYTHEON COMPANY LEXINGTON, MASS. 02173</div> </div>	
		TOLERANCES UNLESS OTHERWISE SPECIFIED	DR. <i>Donald</i> 6 Aug 75		
		FRACTIONS ±	CHK	DRAWING TITLE COMMAND ENCODER TEST SET DEMODULATOR FUNCTIONAL BLOCK DIAGRAM	
		3 PLACE DECIMALS ±	APPROVED <i>Donny</i> 6 May 75		
		2 PLACE DECIMALS ±		SIZE B	CODE IDENT NO. 49956
		1 PLACE DECIMALS ±		DRAWING NO.	
		MATERIAL:	APPROVED	SCALE	SHEET
		NEXT ASSY	BY DIRECTION OF		
		USED ON			
		APPLICATION			

3.1 (Functional Description, Continued)

1. Input crosslink buffer used for all transmission modes
2. Input signal rectification and conditioning for NASA1, NASA2 and NASA6.
3. Zero crossing detection common to NASA3, NASA4, NASA5 and DOD1-13.
4. Register #3 (16 bits) provides first half of frame sync for NASA1 and ratio of subcarrier frequency to data rate for NASA6.
5. Register #4 (16 bits) provides remainder of NASA1 frame sync or NASA5 preset factor representing subcarrier frequencies and bit rate.
6. A common envelope detector is shared by NASA3 and NASA4.
7. A data clock and preset generator function is common to NASA3, NASA4, NASA5 and DOD1-13.
8. A single set of tri-state drivers handles the demodulator data for all transmission modes.

3.2 Design Description

3.2.1 NASA1 (Fig. 3-3)

NASA1 data detection requires synthesizing a phase locked clock to strobe the B1- ϕ -L transmitted signal. Advance knowledge of the sub-carrier frequency and an initialization of one second of ones allows time for a phase locked loop (PLL) to generate the proper frequency, lock onto the incoming data and correct for inverse phasing. Upon proper bit detection, a bit-by-bit search for a frame sync is conducted by comparing programmed 32 bit pattern against the sequence of transmitted data. After detection of frame sync., data bits are accumulated and loaded into registers as 16 bit words for transmission to the microprocessor for evaluation. The NASA1 Demod Flow Chart in Figure 3.4 and Timing Diagram in Figure 3-5 clarify the NASA1 data recovery.

3.2.2 NASA2

The 70KHz FM sub-carrier with 5KHz deviation is transformed by a Frequency to Voltage converter (ref. Fig. 3-6) into the composite of a 1KHz sine wave 100% phase modulated 2KHz sub-carrier. Two threshold detectors establish a counting period for determination of the number of zero crossings derived from a third threshold detector. Each data bit is determined by a logical comparison of the number of zero crossings to the number two. A logic zero will produce one (1) zero crossing whereas a logic one produces three (3) during the counting interval. The termination of an initialization sequence is detected upon receipts of a logic zero following NLT one second of logic ones. Thereafter successive data bits are stored in multiples of five (5) and loaded onto the data bus from a storage register upon request. The NASA2 Flowchart shown in Figure 3-7 and Timing Diagram in Figure 3-8 explain the logical extraction of data.

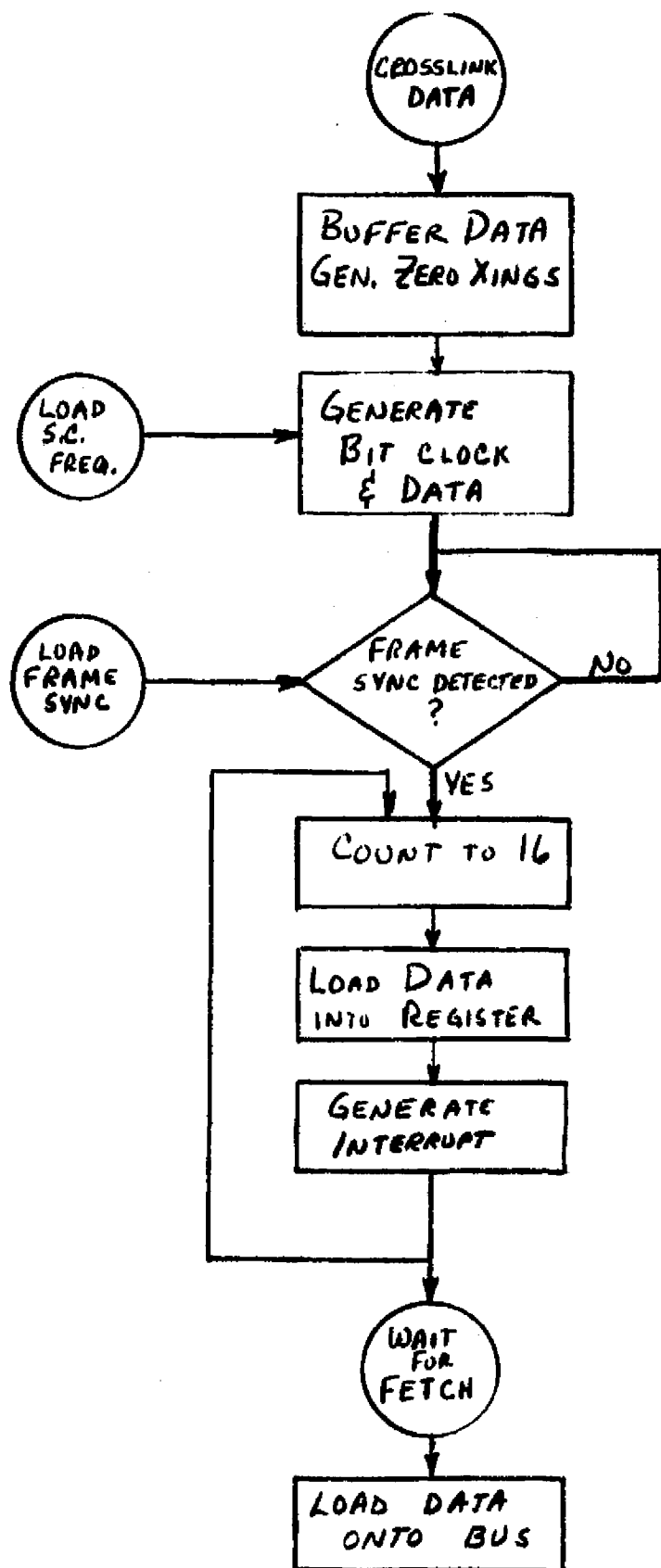
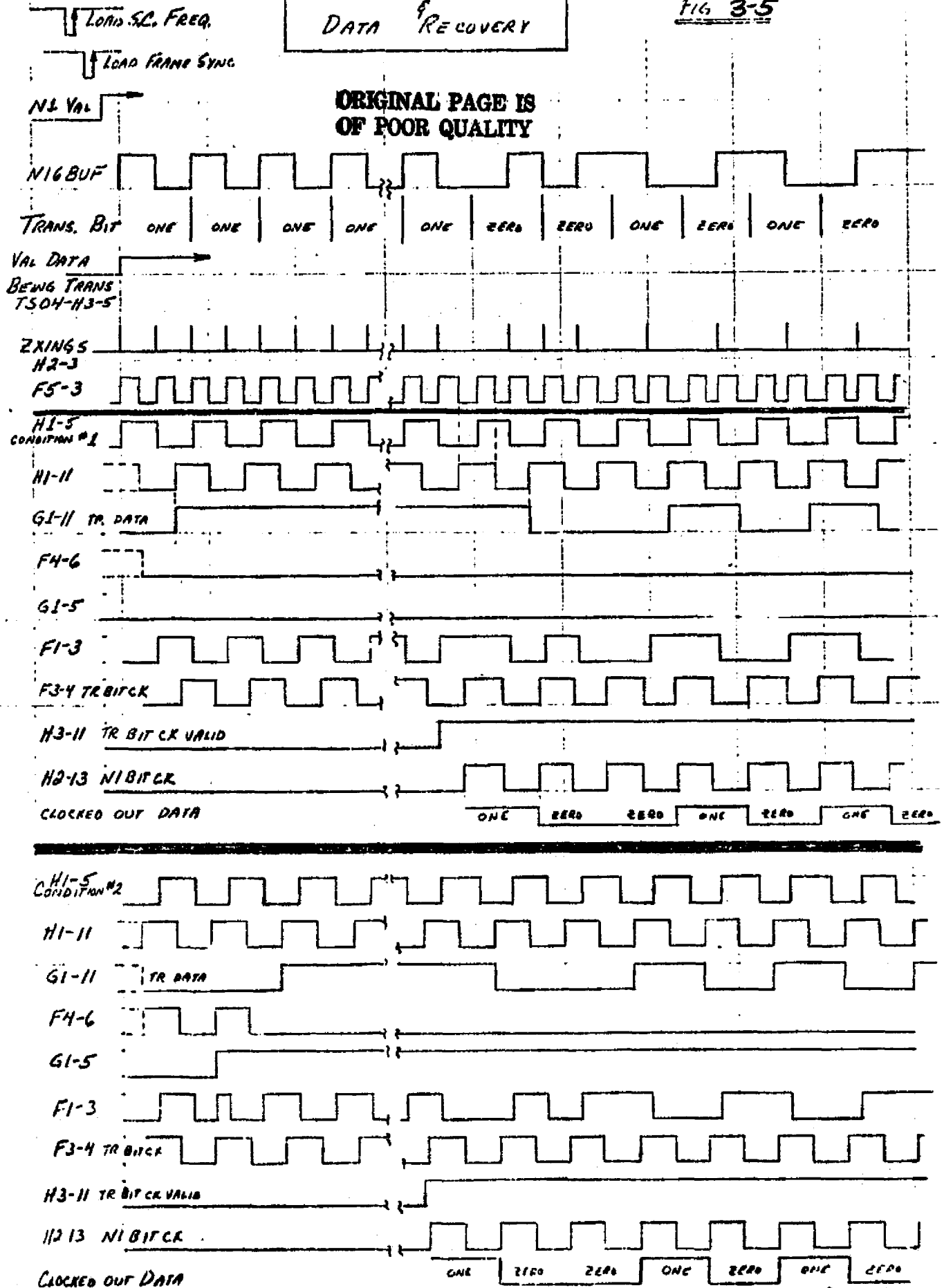


FIGURE 3-4

REV NO.	DR <i>Pewright</i>	DATE <i>5 May '25</i>	CLASSN	<i>Chm</i>
REVISIONS	NASA 1 DEMOD FLOW CHART			
	RAYTHEON	A		REV

NASA 1 & NASA 6
BIT CLOCK GENERATION
DATA RECOVERY

FIG 3-5



5

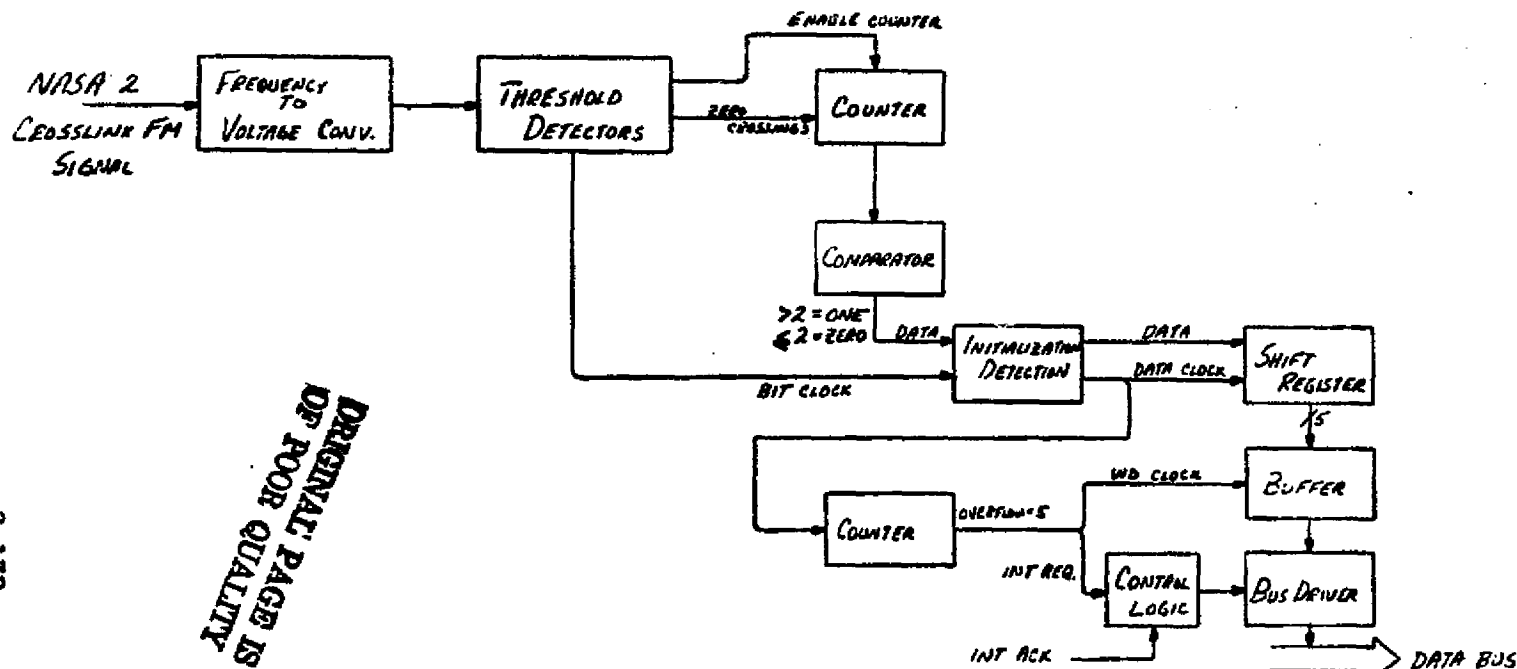
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3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



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PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			CONTR. NO.		
TOLERANCES: ANGLES \pm			DR <i>T. 561</i> 71 <i>Rev. A</i>		
FRACTIONS \pm			CHK		
1 PLACE DECIMALS \pm			A <i>Rev. 48</i> 71 <i>Rev. 75</i>		
2 PLACE DECIMALS \pm			P		
3 PLACE DECIMALS \pm			D		
MATERIAL:			APPROVED		
NEXT ASSY			BY DIRECTION OF		
USED ON			SIZE		
APPLICATION			CODE IDENT NO.		
			DRAWING NO.		
			SCALE		
			SHEET		

RAYTHEON

RAYTHEON COMPANY
LEXINGTON, MASS. 02173DRAWING TITLE
NASA 2 DEMODULATOR
FUNCTIONAL BLOCK DIAGRAMSIZE
BCODE IDENT NO.
49956

DRAWING NO.

Fig 3-6

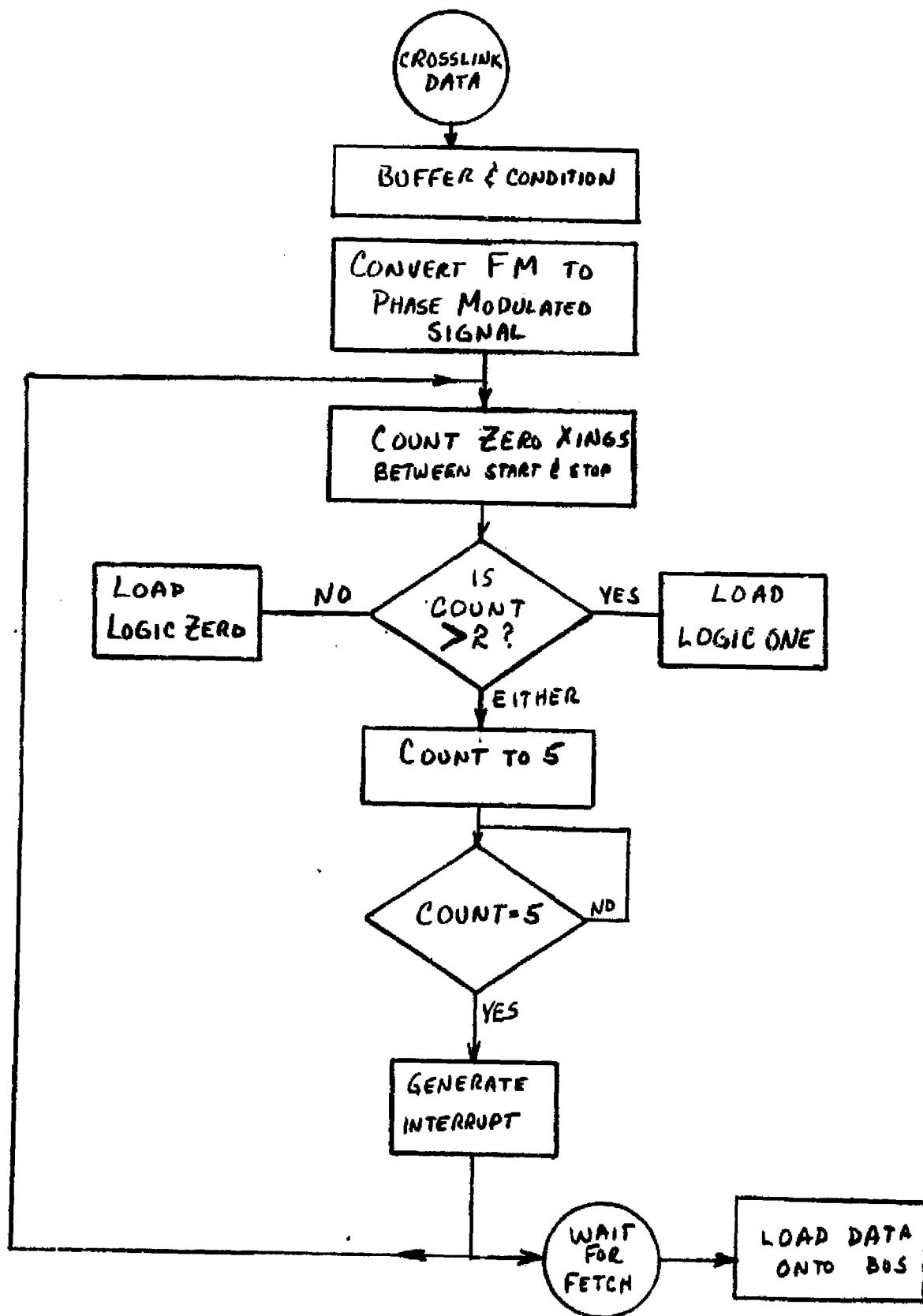
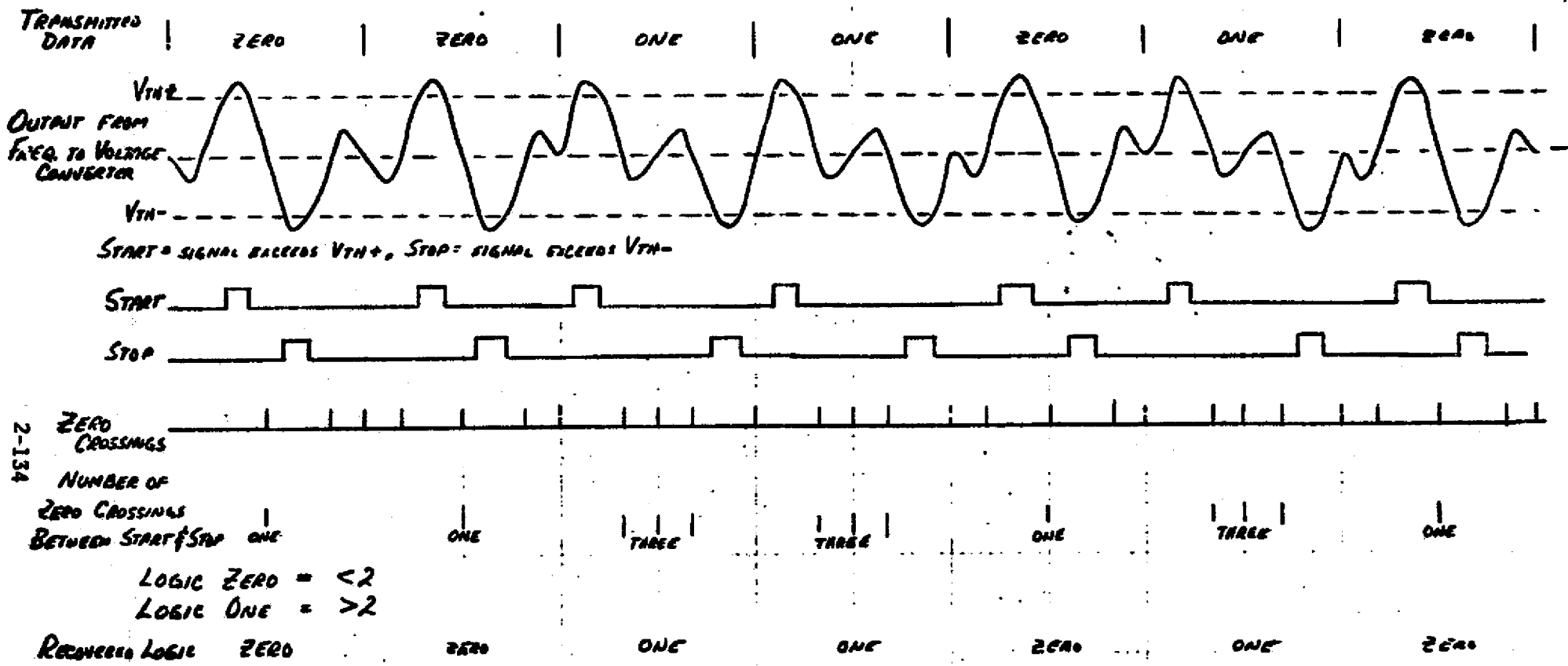


FIGURE 3-7

REV NO	DR <i>Rewright</i>	DATE <i>5 May 73</i>	CLASSN <i>CH</i>
REVISIONS	NASA 2 DEMOD FLOWCHART		
	RAYTHEON		REV



NASA 2
DETECTION

FIGURE 3-8

Rev. 1 28 Feb 75 R

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3.2.3 NASA3

The selection of which of 22 possible frequencies occurs in each tone burst is made by counting the number of zero crossings that occur in a 0.5 second interval (fig. 3-9). In lieu of an accurate timer, the total number of zero crossings is divided by the ratio of the length of the tone burst to one-half second.

Digital comparators sort the measured tone into either an Address or Execute category. A 256 x 4 PROM then selects which of 15 Address tones or which of 7 Execute tones applies (ref. fig. 3-10). A word clock loads the 5 bits defining the frequency of each tone burst into a register for interrogation by the microprocessor. The NASA3 Flowchart and Timing Diagram are shown in figures 3-11 and 3-12, respectively.

3.2.4 NASA4

In order to sort the three possible types of tone burst into a sync., one or zero, the number of zero crossings are counted and digitally compared twice. Detection of a sync. bit inhibits the word clock which loads the one or zero data bits into a register for bit-by-bit evaluation by the microprocessor (refer to figures 3-13, 3-14, and 3-15).

3.2.5 NASA5

Detection of NASA5 data bits requires distinguishing changes in the sub-carrier frequency with the bit times determined by the modulation frequency (refer to figure 3-16, 3-17 and 3-18). Although the phasing of the modulation envelope may vary with respect to the bit times, the peak half of the modulation always occurs within a single bit time. The state of each bit is therefore detected by counting the zero crossings of the sub-carrier during that time of the peak half of the modulation. Comparison of the measured frequency to a preloaded number representing the average of the frequencies for data zero and data one sorts the transmitted data for bit-by-bit evaluation by the microprocessor.

3.2.6 NASA6

NASA6 transmitted data bit detection is comparable to that of NASA1 but with the PLL divided to a programmed frequency corresponding to the NASA6 sub-carrier frequency. Multiples of cycles of the sub-carrier for each bit time occur at a programmed rate. In lieu of a frame sync. pattern, end of the initialization is detected upon receipt of the first logic zero. Data is then accumulated into a 16 bit word as in NASA1 for retrieval and evaluation by the microprocessor (refer to figures 3-19 through 3-22).

3.2.7 DOD1-13

Detection of DOD data requires determining which of three sub-carrier frequencies occur during each bit time (refer to figures 3-23, 3-24 and 3-25). Two bit times occur for each cycle of the triangle modulation of the sub-carrier, which is also skewed with respect to bit time. Although

5

4

3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

D

D

C

C

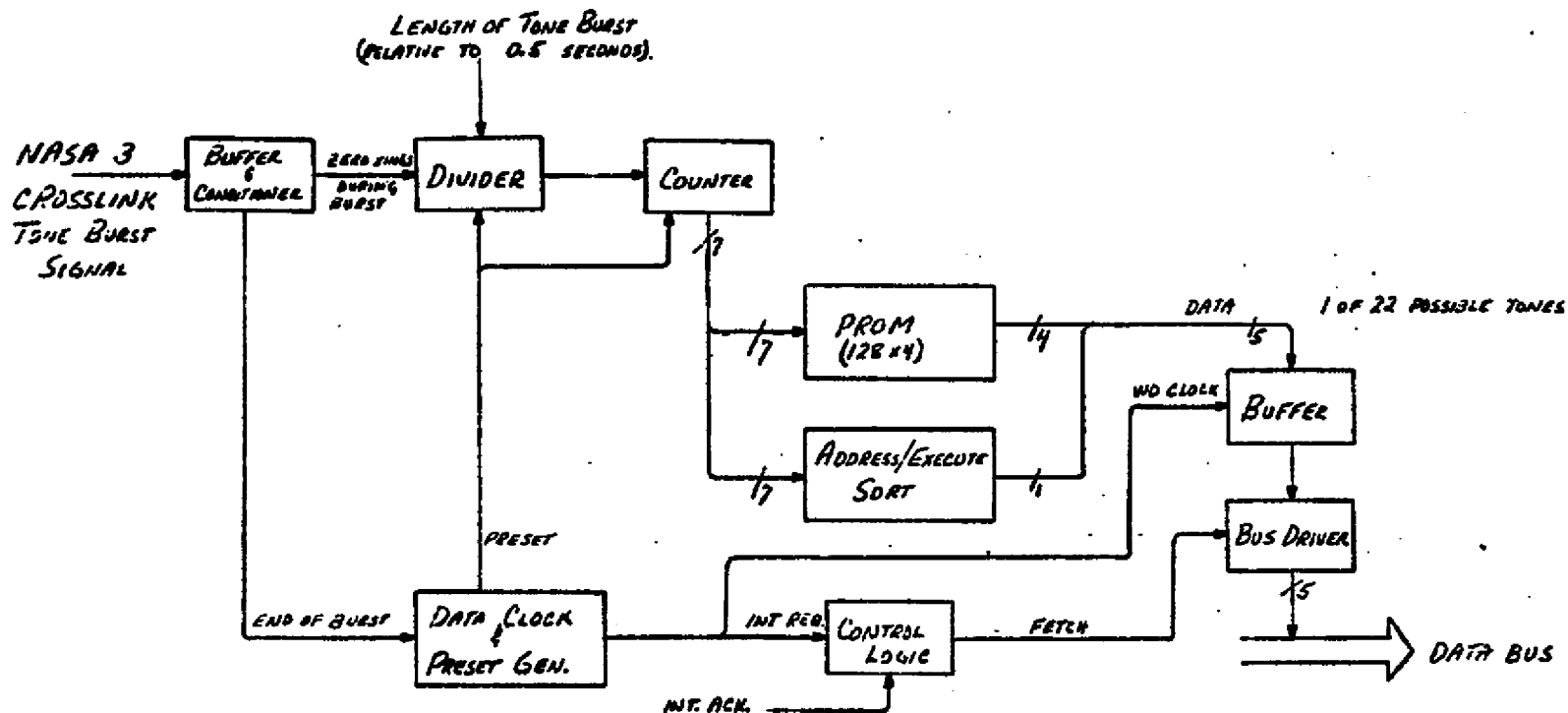
B

B

A

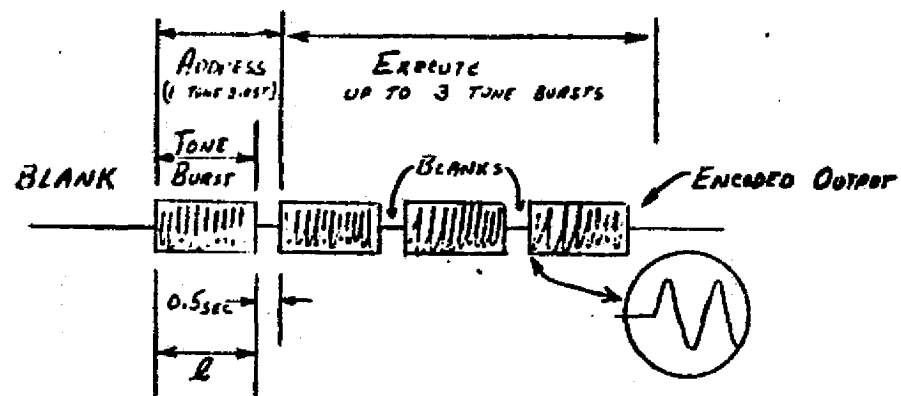
A

2-136



QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			CONTR. NO.		
TOLERANCES: ANGLES ±			DR <i>Leung</i> 28 Nov 75		
FRACTIONS ±			CHK <i>Leung</i> 9 Dec 75		
3 PLACE DECIMALS ±			APPROVED		
2 PLACE DECIMALS ±			BY DIRECTION OF		
1 PLACE DECIMALS ±			MATERIAL:		
NEXT ASSY			USED ON		
APPLICATION			RAYTHEON RAYTHEON COMPANY LEXINGTON, MASS. 02175		
			DRAWING TITLE NASA 3 DEMODULATOR FUNCTIONAL BLOCK DIAGRAM		
			SIZE B CODE IDENT NO. 49956 DRAWING NO. Fig. 3-9		
			SCALE SHEET		

NASA 3 SIGNAL DESCRIPTION



4 BITS (0000 NOT USED) DETERMINE WHICH OF 15 ADDRESS TONES IS GENERATED
3 BITS (000 NOT USED) DETERMINES EXECUTE TONE

TURN ON, TURN OFF AND SELECTION OF TONE TO BE μ CONTROLLER FUNCTION

DURATION OF BLANK (I.E. NO SIGNAL) = 0.5 SEC. (CONSTANT)

DURATION OF TONE BURST = L WHERE L = 0.5, 1.0, 1.5, 2.0, 2.5, 3.0 OR 3.5 SEC (IS SPECIFIED IN BITS 29-31 OF RE COMMAND INSTRUCTION)

ADDRESS CONSISTS OF 1 BURST OF

ONE OF THE FOLLOWING 1025 HZ

1097
1174
1262
1352
1447
1549
1750
1860
4350
4550
5155
5451
5790
6177 HZ

EXECUTE CONSISTS OF UP TO 3 TONE BURSTS OF THE FOLLOWING FREQUENCIES

2000 HZ
2278
2650
3000
3305
3621
3850 HZ

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FIG. 3-10

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Rev. 1 - 21 Feb 75

Rev Feb 75

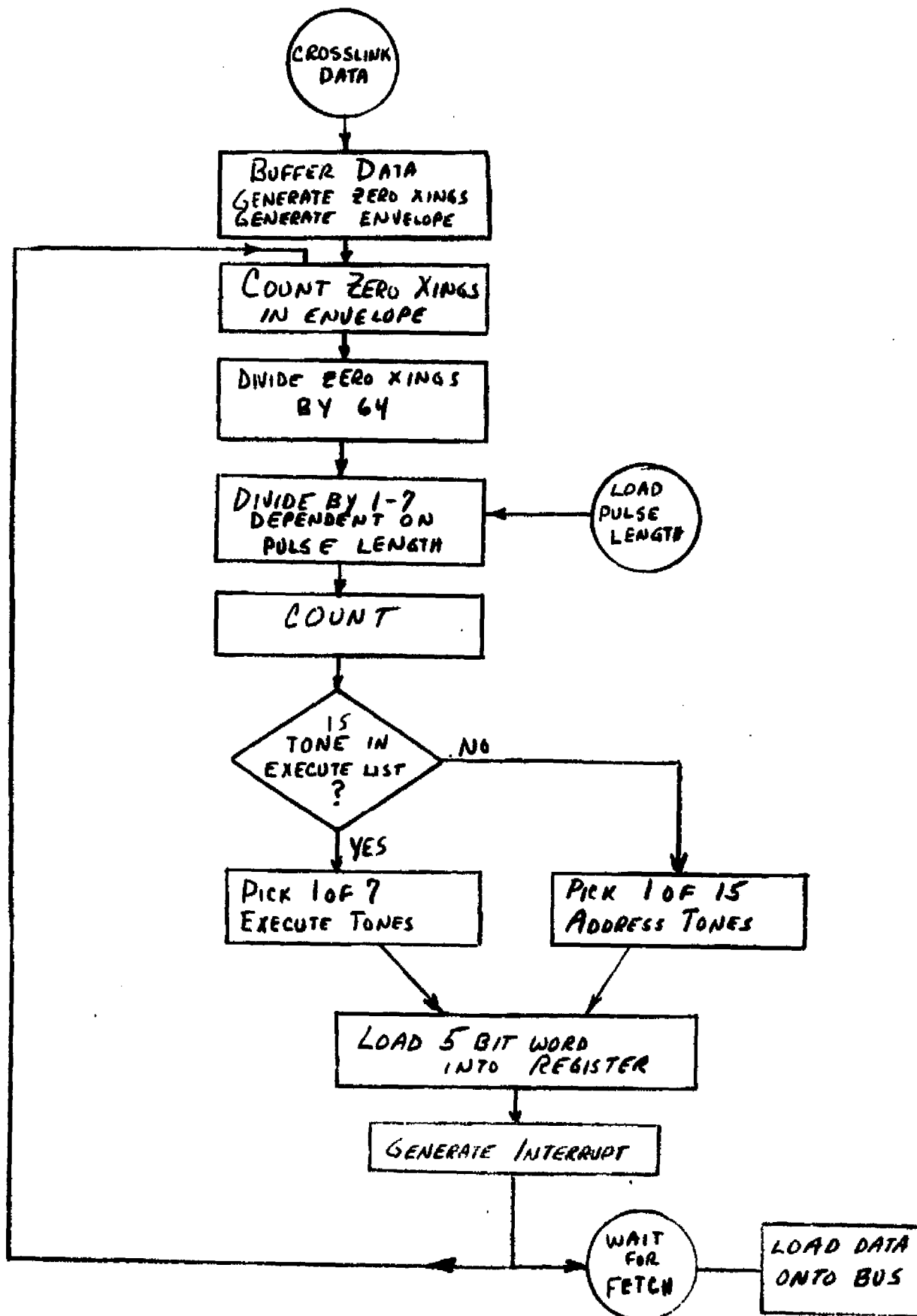


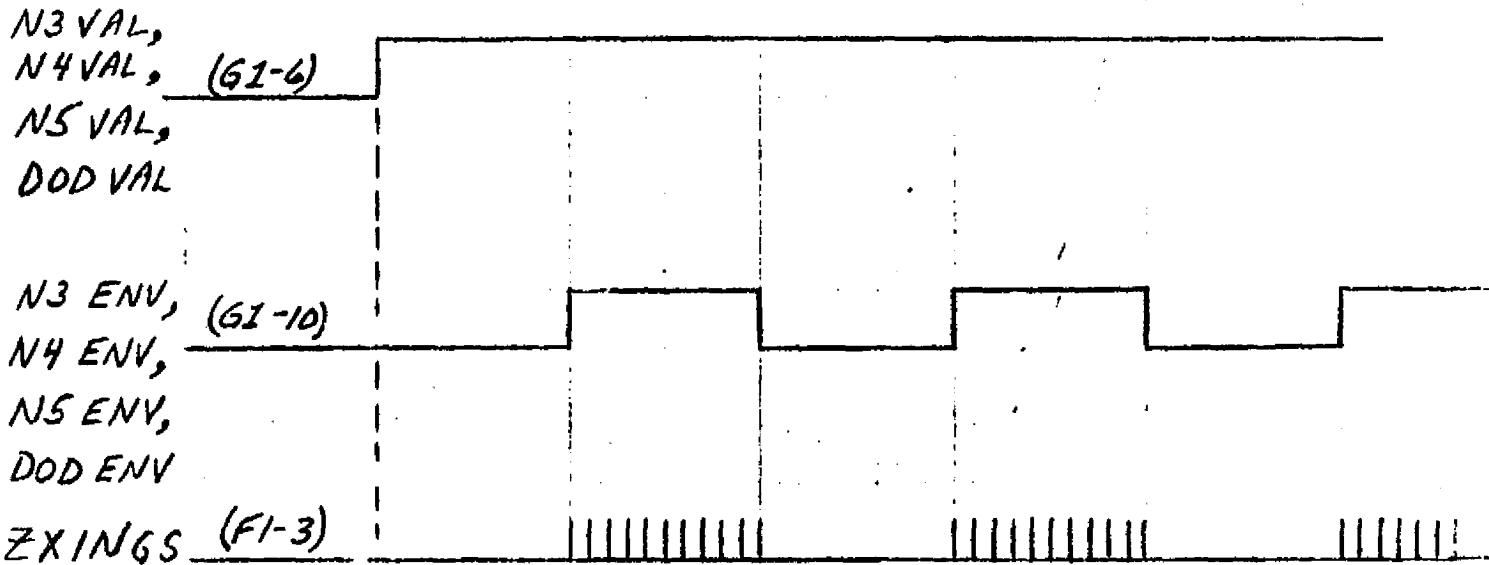
FIGURE 3-11

REV NO	DR <i>Pennell</i>	DATE <i>5 Mar 75</i>	CLASSN <i>CH</i>
	NASA 3 DEMOD FLOW CHART		
	<div style="display: flex; justify-content: space-between;"> <div> </div> <div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div> </div> <div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div> </div> </div>		
REVISIONS	REV		

DATA CLOCK & PRESET GENERATOR
(N3-N4-N5-DOD)
TIMING DIAGRAM

REF. DWG 893208 SHEET 1 OF 5

INPUTS



OUTPUTS

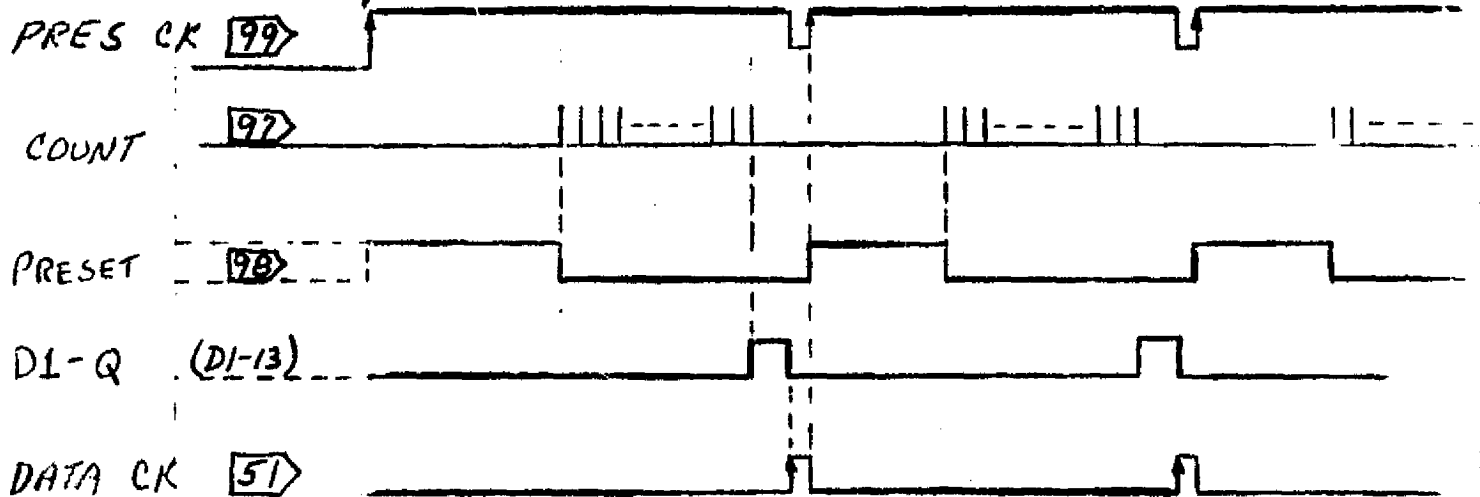


Fig. 3-12

5

4

3

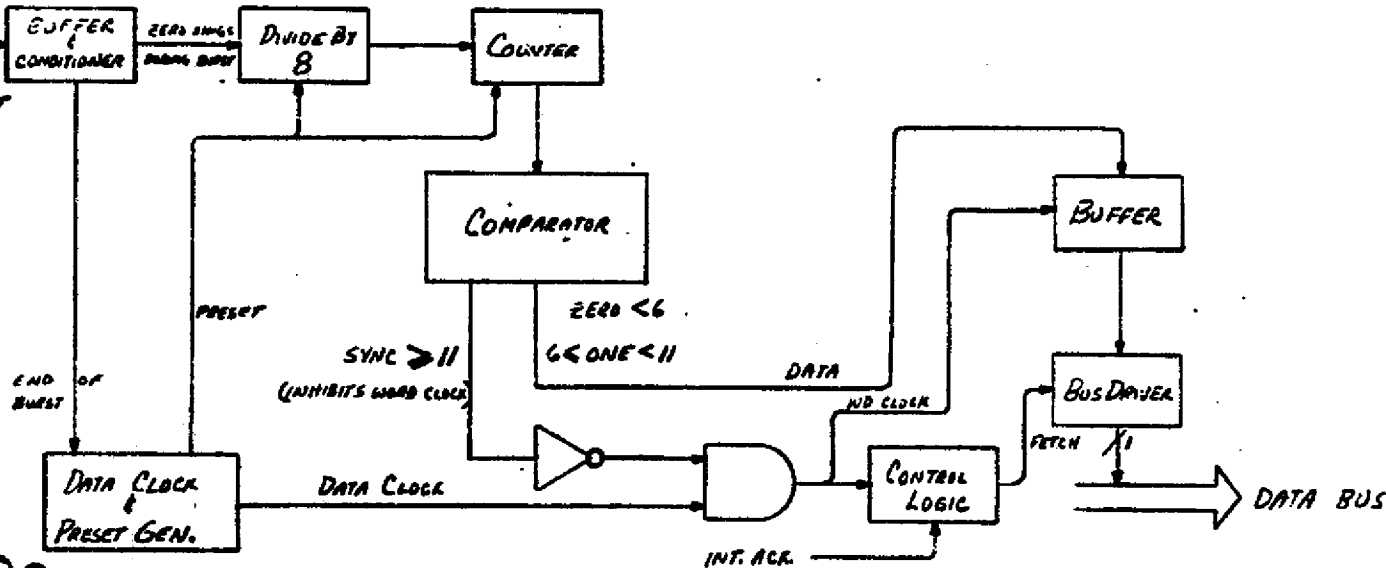
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1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

LOGIC ZERO = 36 ZERO CROSSINGS
 LOGIC ONE = 72 ZERO CROSSINGS
 LOGIC SYNC = 108 ZERO CROSSINGS

NASA 4
 CROSSLINK
 TONE BURST



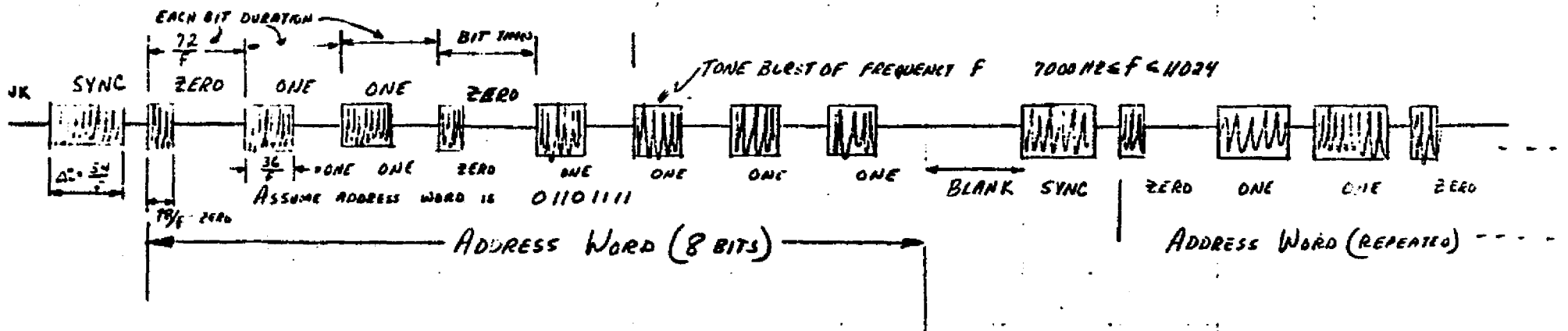
2-140

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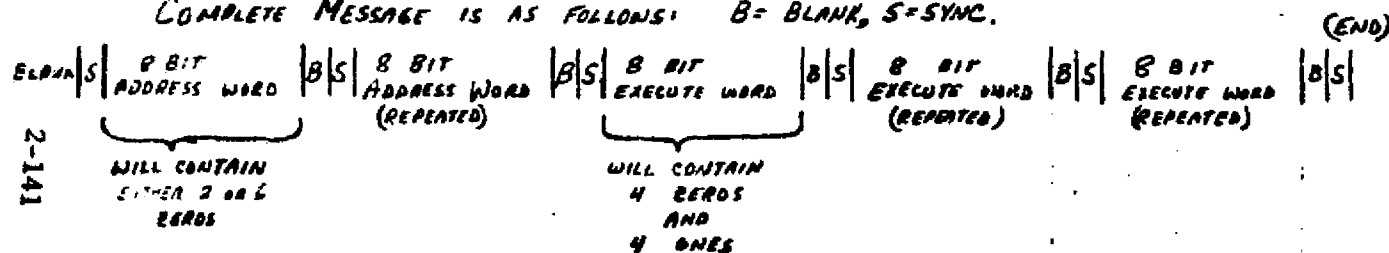
QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	FINO NO
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			CONTR NO.		
TOLERANCES: ANGLES \pm			DR <i>1/10/60</i> 27001		
FRACTIONS \pm			CHK <i>1/10/60</i> 12001/15		
3 PLACE DECIMALS \pm			APPROVED		
2 PLACE DECIMALS \pm			BY DIRECTION OF		
1 PLACE DECIMALS \pm			MATERIAL:		
NEXT ASSY			USED ON		
APPLICATION			RAYTHEON RAYTHEON COMPANY LEXINGTON, MASS. 02173		
			DRAWING TITLE NASA 4 DEMODULATOR FUNCTIONAL BLOCK DIAGRAM		
			SIZE B CODE IDENT NO. 49956 DRAWING NO. 3-13		
			SCALE SHEET		

NASA 4 SIGNAL DESCRIPTION

EXPANDED PORTION OF MESSAGE



COMPLETE MESSAGE IS AS FOLLOWS: B=BLANK, S=SYNC.



Summary:

A. 4 POSSIBLE SYMBOLS TRANSMITTED

1. BLANK - NO SIGNAL
2. SYNC - 54 CYCLES OF SUB CARRIER
3. ONE - 36 CYCLES OF SUB CARRIER
4. ZERO - 18 CYCLES OF SUB CARRIER

B. FREQUENCY OF SUB CARRIER FIXED IN RANGE FROM 7000 HZ TO 11024 HZ

TIME DURATION OF PULSE AND BLANKS.
CONTROLLED BY NFM REGISTERS IN
MODULATOR

FIGURE 3-14

Rev 1 11 Mar 75

REN:75:70 Ren 17 Feb '75

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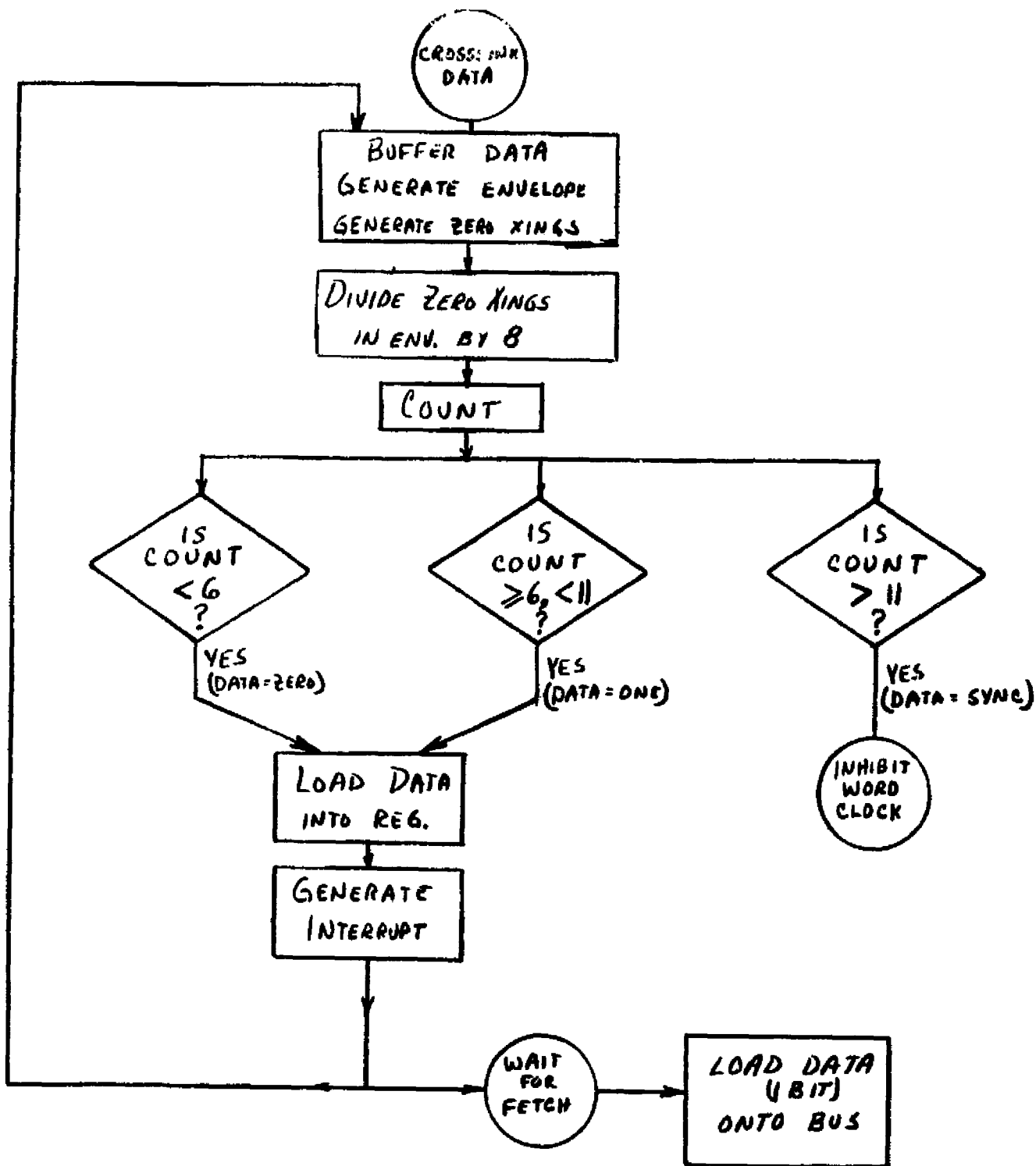


FIGURE 3-15

REV NO.	DR <i>Amright</i>	DATE <i>May '75</i>	CLASSN <i>CH</i>
	NASA 4 DEMOD FLOW CHART		
REVISIONS	RAYTHEON	F	REV

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4

3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NASA 5
CROSSLINKBuffer
Conditioner

COUNTER

COMPARATOR

COUNT < PRELOAD = LOGIC ONE, (LOWEST FREQ.)
 COUNT > PRELOAD = LOGIC ZERO (HIGHEST FREQ.)

BUFFER

BUS
DRIVER

DATA BUS

PRELOAD
 MEAN NO. OF ZERO CROSSINGS
 OF LOGIC ONE AND ZERO
 DURING 1/2 BIT TIME

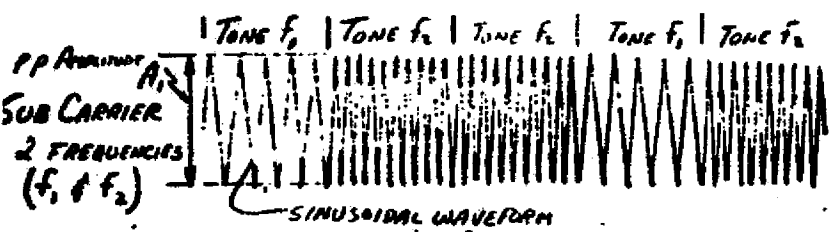
PRESET

DATA CLOCK
&
PRESET GEN.CONTROL
LOGIC

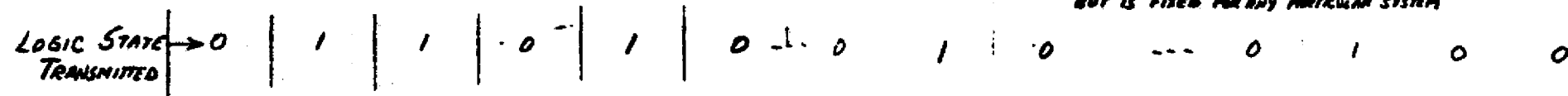
2-143

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PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CONTR. NO.		RAYTHEON RAYTHEON COMPANY LEXINGTON, MASS. 02173	
TOLERANCES: ANGLES ±		DR <i>Revised</i>	DATE <i>5-2-71</i>	DRAWING TITLE <i>NASA 5 DEMODULATOR</i>	
FRACTIONS ±		CHK <i>Revised</i>	DATE <i>12 May 72</i>	FUNCTIONAL BLOCK DIAGRAM	
3 PLACE DECIMALS ±		APPROVED		SIZE B	CODE IDENT NO. 49956
2 PLACE DECIMALS ±		BY DIRECTION OF		DRAWING NO. <i>Fig. 3-16</i>	
1 PLACE DECIMALS ±				SCALE	SHEET
MATERIAL:					
NEXT ASSY	USED ON				
APPLICATION					



TONE F_1 CORRESPONDS TO A LOGIC 0
 TONE F_2 CORRESPONDS TO A LOGIC 1
 TWO TONES ASSIGNED IN RANGE FROM 7KHZ TO 21KHZ

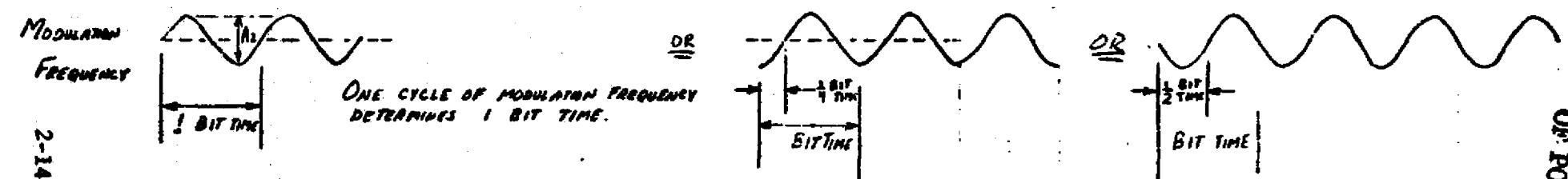
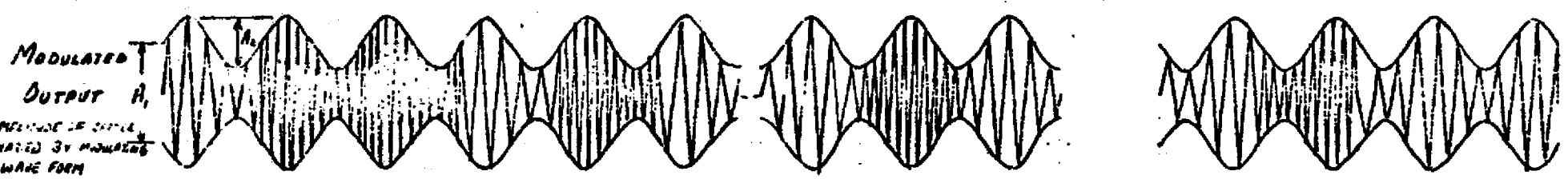


FOR 50% AMPLITUDE MODULATION, A_2 AMPLITUDE (MODULATION AMPLITUDE) = $0.5 A_1$ AMPLITUDE (SUBCARRIER AMPLITUDE)

COMPLETE NASA 5 COMMAND FORMAT

INITIALIZATION		MESSAGE		TERMINATION
≥ 13 ZEROS	1 UM	7 BITS ADDRESS	8 - n COMMAND	≥ 20 ZEROS

WHERE n IS AN INTEGER $7 \leq n \leq 64$
 BUT IS FIXED FOR ANY PARTICULAR SYSTEM



DELAY OF POSITIVE GOING, ZERO CROSSING OF MODULATION FREQUENCY WITH RESPECT TO BIT TIME MAY BE 0 (COINCIDENT), $1/4$ BIT TIME OR $1/2$ BIT TIME. THIS WILL BE FIXED FOR ANY GIVEN VEHICLE (SYSTEM).

MODULATION FREQUENCIES ALLOWABLE (FIXED FOR EACH PARTICULAR SYSTEM) ARE 2^i BITS/SEC WHERE i IS AN INTEGER $3 \leq i \leq 10$ AND $100 \cdot 2^i$ BITS/SEC WHERE i IS AN INTEGER $1 \leq i \leq 12$

NASA 5
 SIGNAL DESCRIPTION

FIGURE 3-17

REW: 7510

Rev 282

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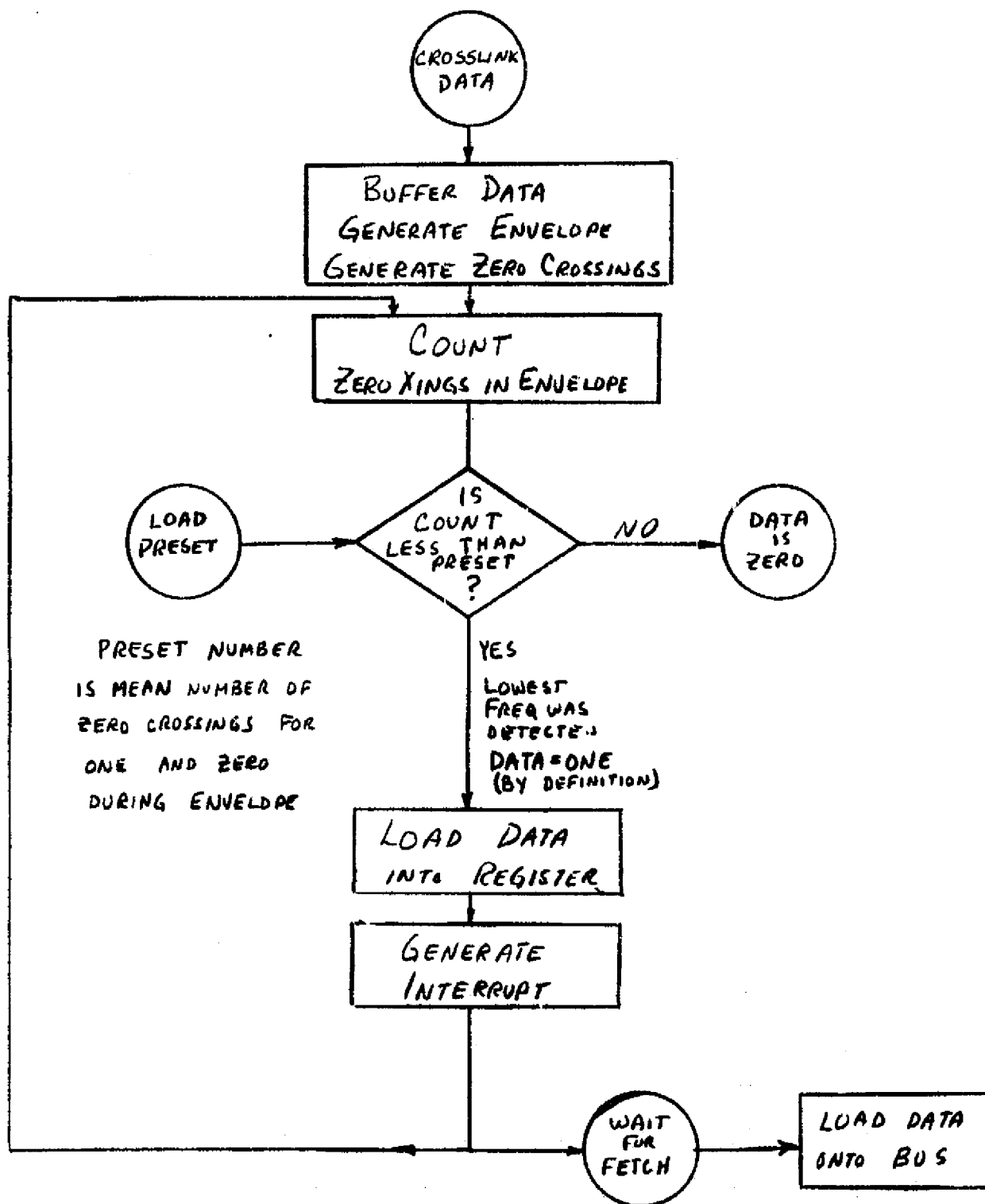
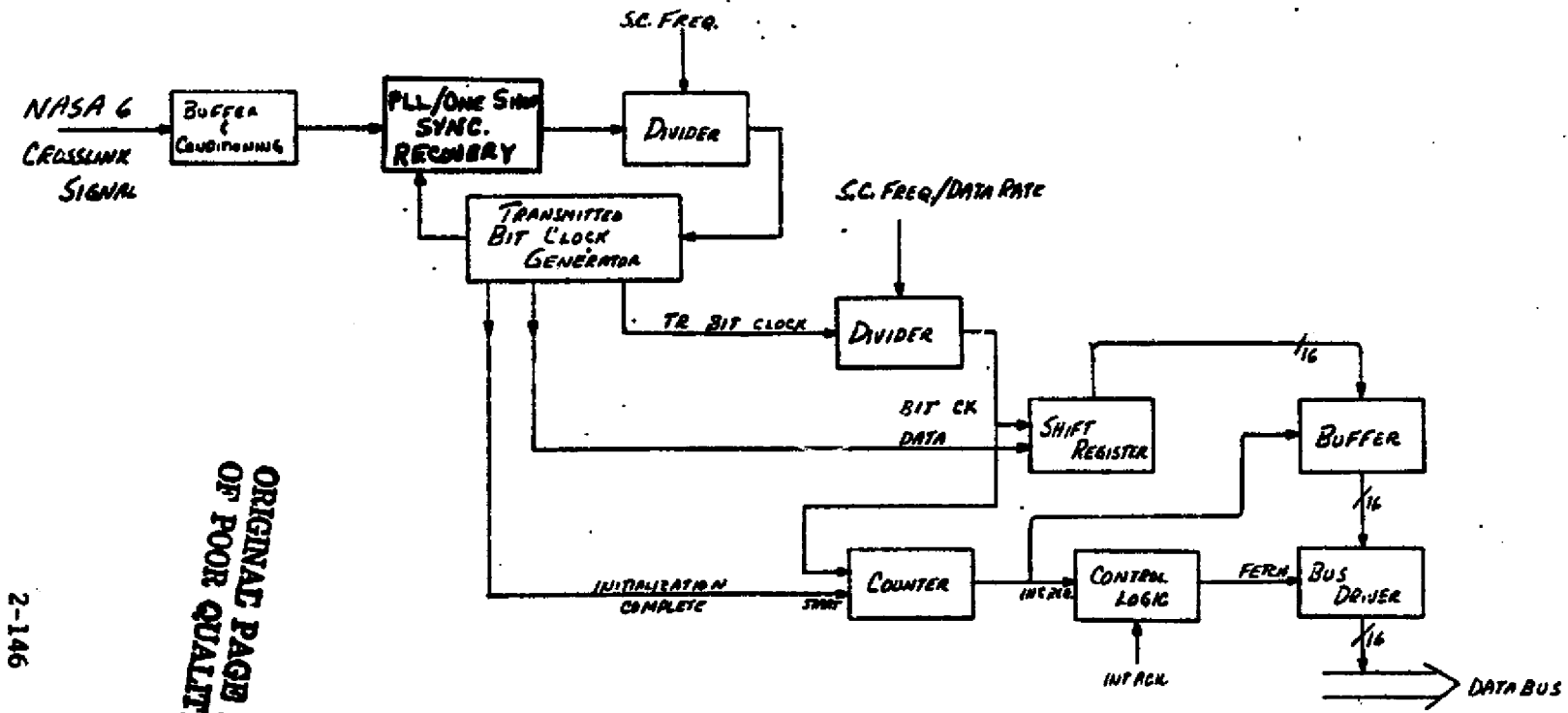


FIGURE 3-18

REVISIONS	DR <i>Hemight</i>	DATE <i>6 May 75</i>	CLASSN <i>CM</i>
	NASA 5 DEMOD FLOW CHART		
	<div style="display: flex; justify-content: space-between;"> <div>RAYTHEON</div> <div>REV</div> </div>		

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MOD.		IDENT NO.		IDENTIFICATION NO.		SPECIFICATION NO.		DESCRIPTION		NO.																																											
<table border="1"> <tr> <td colspan="2">CONTR. NO.</td> <td colspan="2">RAYTHEON</td> <td colspan="2">RAYTHEON COMPANY</td> </tr> <tr> <td colspan="2">DR. <i>Boyd</i></td> <td colspan="2">CHK. <i>Boyd</i></td> <td colspan="2">LEXINGTON, MASS. 02173</td> </tr> <tr> <td colspan="2">APPROVED</td> <td colspan="2">DRAWING TITLE</td> <td colspan="2">NASA 6 DEMODULATOR</td> </tr> <tr> <td colspan="2">BY DIRECTION OF</td> <td colspan="2">FUNCTIONAL BLOCK DIAGRAM</td> <td colspan="2"></td> </tr> <tr> <td colspan="2">SIZE</td> <td colspan="2">CODE IDENT NO.</td> <td colspan="2">DRAWING NO.</td> </tr> <tr> <td colspan="2">B</td> <td colspan="2">49956</td> <td colspan="2">Fig. 3-19</td> </tr> <tr> <td colspan="2">SCALE</td> <td colspan="2"></td> <td colspan="2">SHEET</td> </tr> </table>												CONTR. NO.		RAYTHEON		RAYTHEON COMPANY		DR. <i>Boyd</i>		CHK. <i>Boyd</i>		LEXINGTON, MASS. 02173		APPROVED		DRAWING TITLE		NASA 6 DEMODULATOR		BY DIRECTION OF		FUNCTIONAL BLOCK DIAGRAM				SIZE		CODE IDENT NO.		DRAWING NO.		B		49956		Fig. 3-19		SCALE				SHEET	
CONTR. NO.		RAYTHEON		RAYTHEON COMPANY																																																	
DR. <i>Boyd</i>		CHK. <i>Boyd</i>		LEXINGTON, MASS. 02173																																																	
APPROVED		DRAWING TITLE		NASA 6 DEMODULATOR																																																	
BY DIRECTION OF		FUNCTIONAL BLOCK DIAGRAM																																																			
SIZE		CODE IDENT NO.		DRAWING NO.																																																	
B		49956		Fig. 3-19																																																	
SCALE				SHEET																																																	
<table border="1"> <tr> <td colspan="2">MATERIAL:</td> <td colspan="2">APPLICATION</td> </tr> <tr> <td colspan="2">NEXT ASSY</td> <td colspan="2">USED ON</td> </tr> </table>												MATERIAL:		APPLICATION		NEXT ASSY		USED ON																																			
MATERIAL:		APPLICATION																																																			
NEXT ASSY		USED ON																																																			

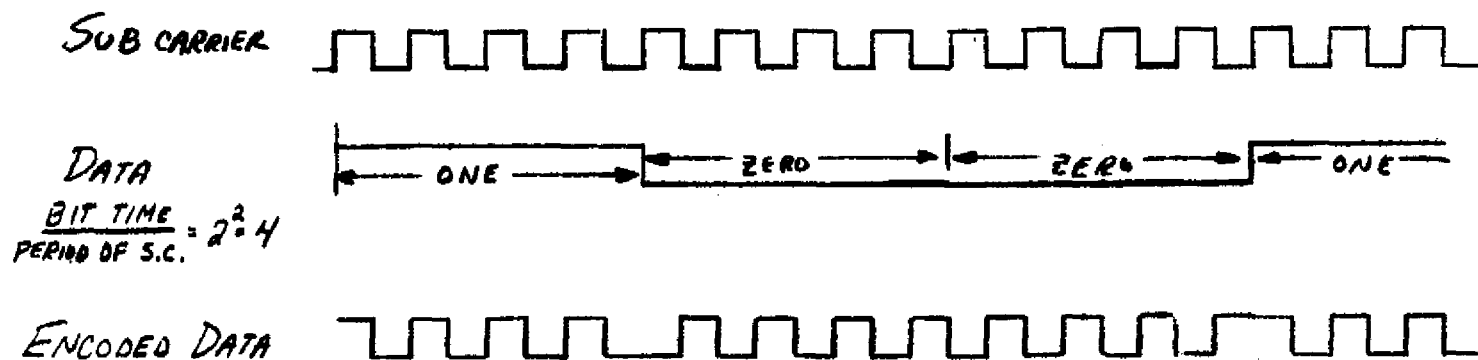
NASA 6 (GENERALIZED NASA 1)

in NASA 1 (BI-φ-L), $\frac{\text{BIT TIME}}{\text{PERIOD OF SUB CARRIER}} = 2^0 = 1$
 in NASA 6:

$$2^1 \leq \frac{\text{BIT TIME}}{\text{PERIOD OF SUB CARRIER}} \leq 2^4 (2048)$$

$$2^1 \leq \text{FREQUENCY OF SUB CARRIER (SQ. WAVE.)} \leq 2^{12} (4096 \text{ Hz})$$

$$2^0 \leq \text{FREQUENCY OF DATA BITS} \leq 2^4 (2048 \text{ Hz})$$



NASA 6 SIGNAL DESCRIPTION

FIGURE 3-20

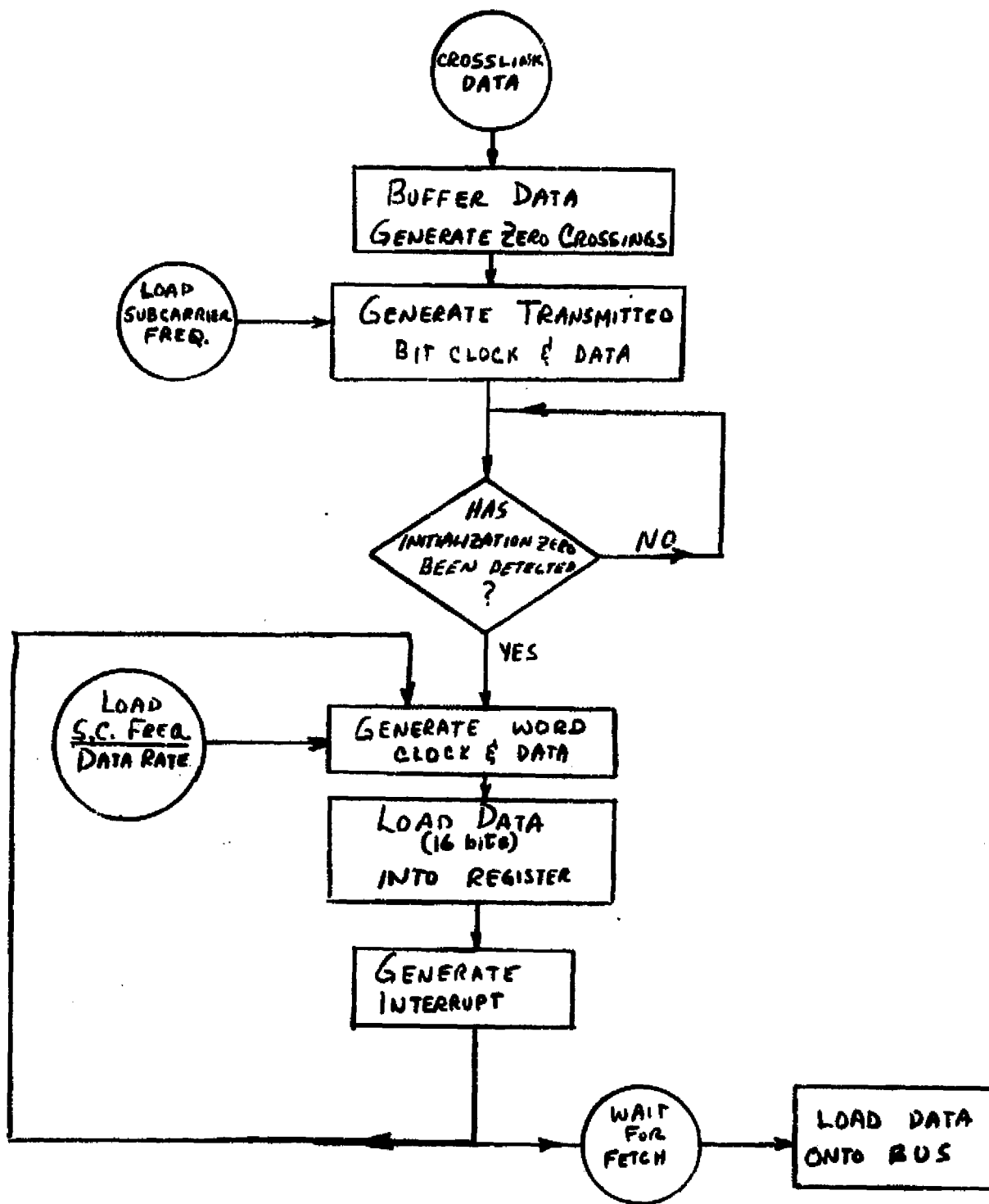


FIGURE 3-21

REV NO	DR <i>Amv</i>	DATE <i>6 May 73</i>	CLASSN <i>C-11</i>
REVISIONS	NASA 6 DEMOD FLOW CHART		
	RAYTHEON		REV

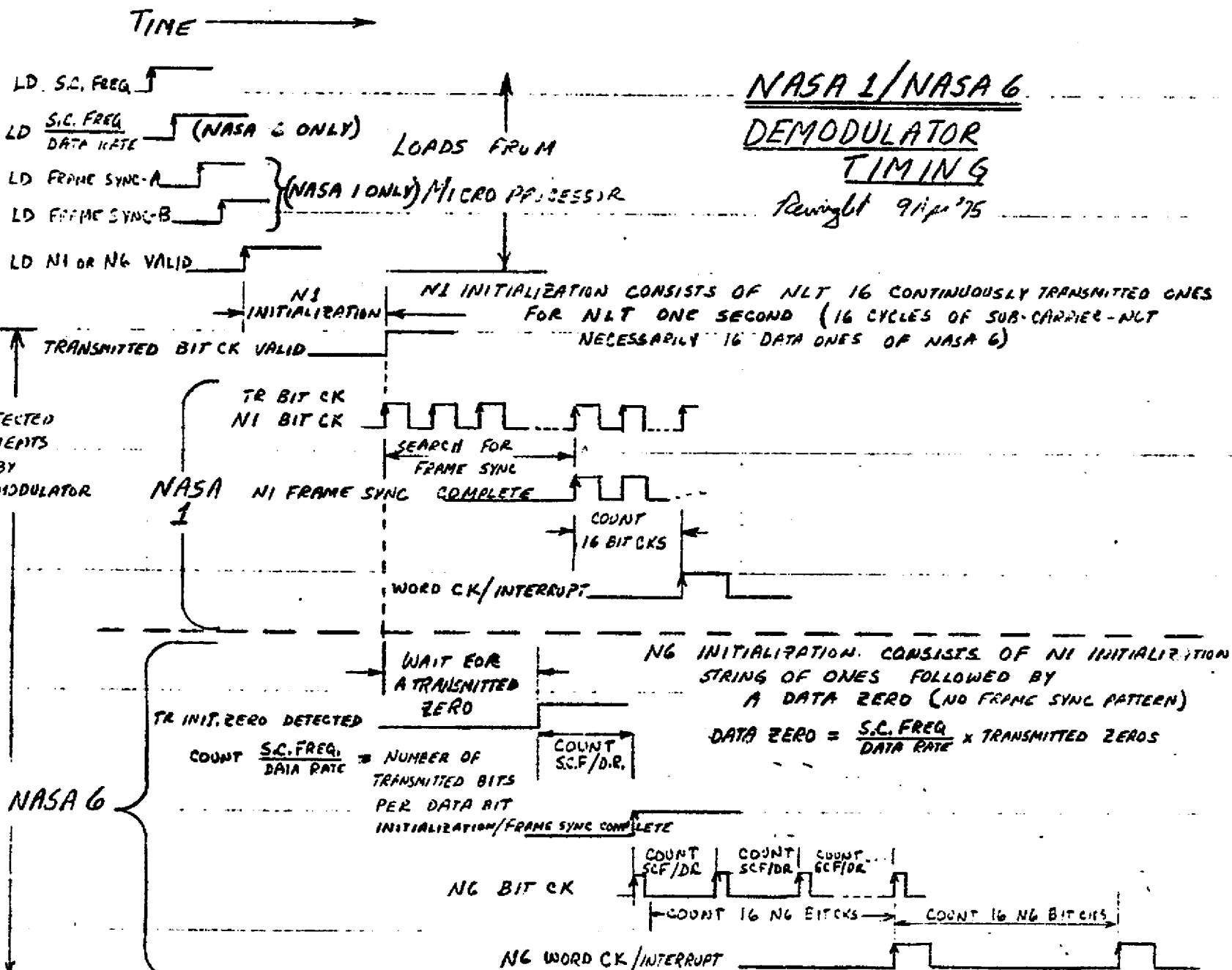


Fig 3-22

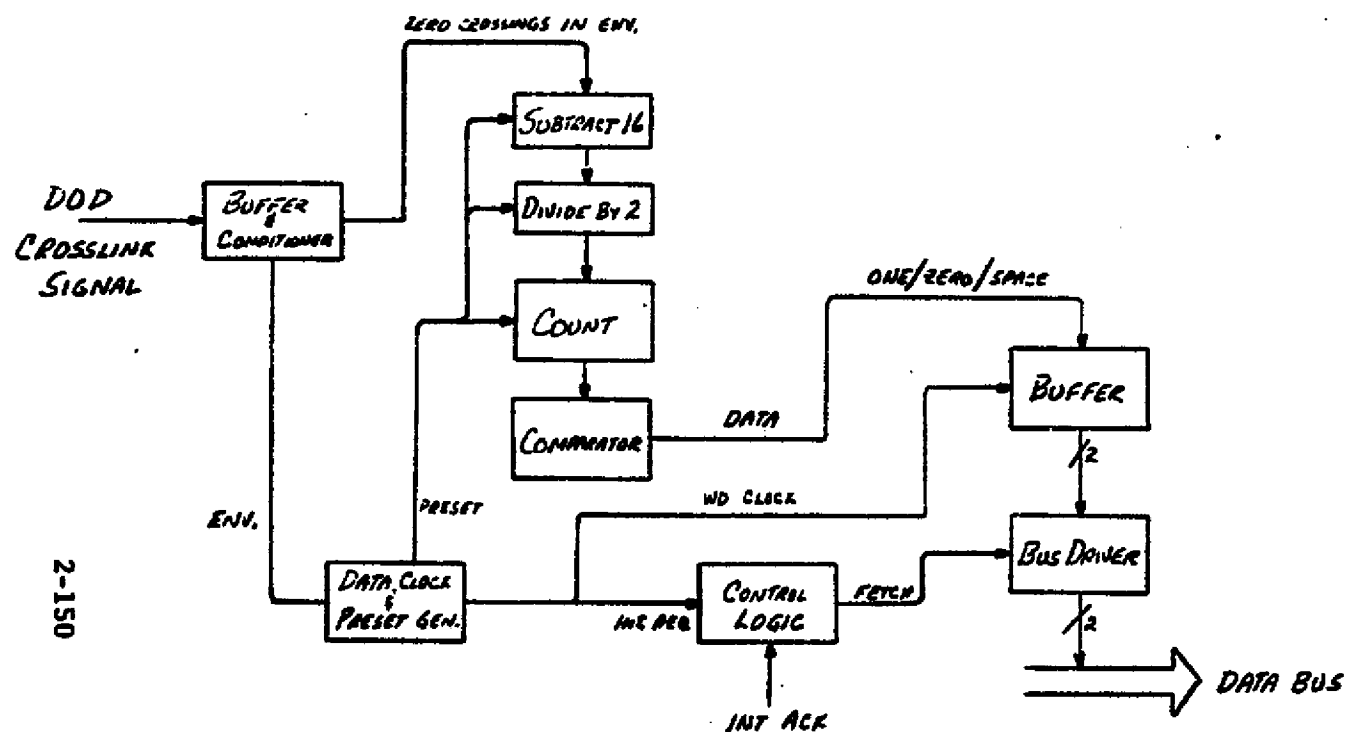
5

4

3

2

1



QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.
PARTS LIST					
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR. NO.		
		TOLERANCES: ANGLES \pm	DR <i>Thurgt</i> <i>Mar. 71</i>		
		FRACTIONS \pm	CHK		
		3 PLACE DECIMALS \pm	A <i>Thurgt</i> <i>6 May 75</i>		
		2 PLACE DECIMALS \pm	P		
		1 PLACE DECIMALS \pm	D		
		MATERIAL:	APPROVED		
NEXT ASSY	USED ON		BY DIRECTION OF		
APPLICATION			SIZE B CODE IDENT NO. 49956 DRAWING NO. <i>Fig. 3-23</i>		
			SCALE SHEET		

RAYTHEON

RAYTHEON COMPANY
LEXINGTON, MASS. 02173DRAWING TITLE *DOD DEMODULATOR
FUNCTIONAL BLOCK DIAGRAM*SIZE B CODE IDENT NO. 49956 DRAWING NO. *Fig. 3-23*

SCALE SHEET

SPACE FREQUENCY = 65 KHZ
 ZERO FREQUENCY = 76 KHZ
 ONE FREQUENCY = 95 KHZ

FREQUENCY OF SUB CARRIER VARIES WITH DESIRED LOGIC STATE (3)



LOGIC STATES | SPACE | SPACE | SPACE | SPACE | SPACE | ONE | ZERO | ONE | SPACE | ZERO | SPACE | ONE |

TRIANGULAR
 MODULATION
 FREQUENCY
 500 HZ OR 1 KHZ

POSITIVE GOING ZERO CROSSOVER

FOR 50% AMPLITUDE MODULATION, A_2 AMPLITUDE = 0.5 A_1 AMPLITUDE

BIT RATE = 1 KB/S OR 2 KB/S = 2 * MOD. FREQ.

AMPLITUDE OF SUB CARRIER
 IS VARIED BY THE TRIANGULAR
 MODULATION FREQUENCY.

MODULATED
 OUTPUT

SUM OF SUBCARRIER
 AND
 TRIANGLE MODULATION
 FREQUENCIES

DOD 1-13
 SIGNAL DESCRIPTION

FIGURE 3-24

REVISED TO
 RGS. 141M4.

Rev 18 Feb 75

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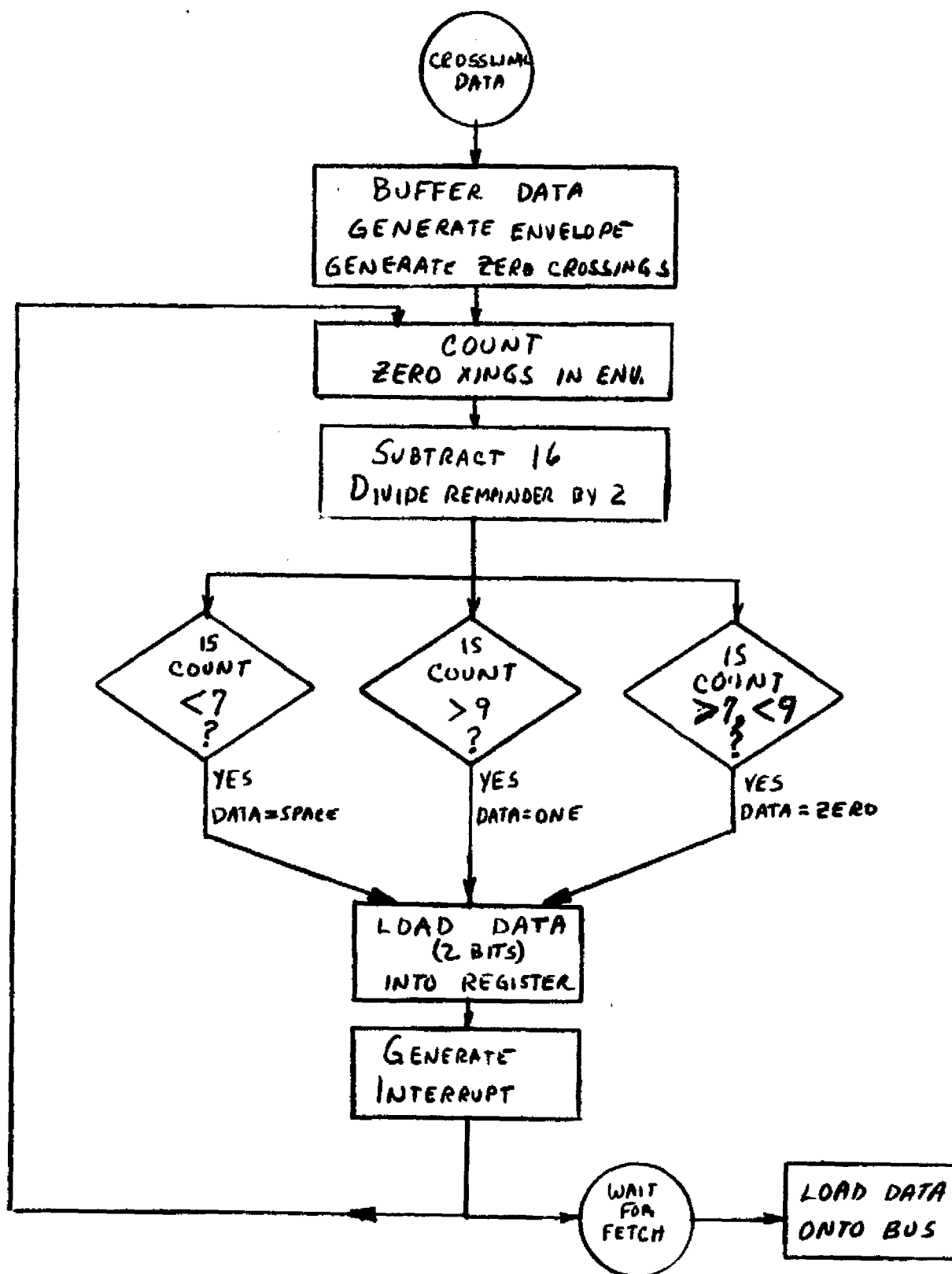


FIGURE 3-25

REVISIONS	REV NO	DR <i>Reynolds</i>	DATE <i>6/10/58</i>	CLASSN <i>CTR</i>
	DOD DEMOD FLOW CHART			
	<div style="display: flex; justify-content: space-between;"> <div>RAYTHEON</div> <div></div> <div></div> </div>			

RAYTHEON COMPANY

EQUIPMENT DIVISION

RAYTHEON

3.2.7 (DOD1-13, Continued)

the modulation frequency may be either 500Hz or 1KHz, both zero cross-overs (i.e. the positive going and the negative going) occur 6/10ths of the way into a bit time. The resultant 4/10ths of a bit time, or NLT 200 microseconds, is used to sample the sub-carrier frequency each bit time. Two data lines, representing space, one or zero are clocked into registers for bit-by-bit sampling by the microprocessor.

3.3 Initialization Requirements (Refer to Fig. 3-26)

3.3.1 NASA1 with Voice (40.330 KHz)

ADDRESS	NAME	DATA (OCTAL)
1. 176141	Load S.C. Freq.	000367
2. 176143	Load Reg. 4	First 16-bits of Frame Sync* (MSB = CBD15, LSB = CBD00)
3. 176142	Load Reg. 3	Remainder of Frame Sync*
4. 176140	Load Control Reg.	100000

*Cannot be all ones

3.3.2 NASA1 without Voice (8.066 KHz)

ADDRESS	NAME	DATA (OCTAL)
1. 176141	Load S.C. Freq.	000267
2. 176143	Load Reg. 4	First 16-bits of Frame Sync*
3. 176142	Load Reg. 3	Remainder of Frame Sync
4. 176140	Load Control Reg.	100000

3.3.3 NASA2

1. 176140	Load Control Reg.	040000
-----------	-------------------	--------

3.3.4 NASA3

1. 176140	Load Control Reg.	TONE LENGTH	DATA
		0.5 sec.	020740
		1.0 sec.	020700
		1.5 sec.	020640
		2.0 sec.	020600
		2.5 sec.	020540
		3.0 sec.	020500
		3.5 sec.	020440

DEMODULATOR REGISTER & ADDRESSES DATA FORMATS

	ADDRESS	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAD'S	176140	CONTROL REG.	N1	N2	N3	N4	N5	N6	DOD	TONE	← N3 →	LENGTH	TEST		X	X	X	X
	176141	N1/N6 S.C. FREQ.	MSB															LSB
	176142	REGISTER 3																
	176143	REGISTER 4																
	176144	TEST DATA																
	176145	TEST CLOCK																
READ'S	176147	DATA WORD																
		NASA 1	MSB	←														→ LSB
		NASA 2	X	X	X	X	X	X	X	X	X	X	X	MSB	←			→ LSB
		NASA 3	X	X	X	MSB	←					LSB	X	X	X	X	X	X
		NASA 4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DATA
		NASA 5	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DATA
		NASA 6	MSB	←														→ LSB
		DOD 1-13	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DATA	1/0

X = AMBIGUOUS/DONT CARE

FIGURE 3-26

RAYTHEON COMPANY

RAYTHEON

ADDRESS	NAME	DATA (OCTAL)																										
3.3.5 <u>NASA4</u>																												
1. 176140	Load Control Reg.	010000																										
3.3.6 <u>NASA5</u>																												
1. 176143	Load Reg. 4	$\frac{F_1 + F_2}{2(\text{bit rate})} \quad (F_1, F_2, \text{Bit Rate in hertz})$ with LSB = 2^0 MSB = 2^{10}																										
2. 176140	Load Control Reg.	004000																										
3.3.7 <u>NASA6</u>																												
1. 176141	Load S.C. Freq.	<table><tr><th><u>S.C. FREQ.</u></th><th><u>DATA</u></th></tr><tr><td>4096</td><td>000373</td></tr><tr><td>2048</td><td>000353</td></tr><tr><td>1024</td><td>000313</td></tr><tr><td>512</td><td>000213</td></tr><tr><td>256</td><td>000375</td></tr><tr><td>128</td><td>000355</td></tr><tr><td>64</td><td>000315</td></tr><tr><td>32</td><td>000215</td></tr><tr><td>16</td><td>000356</td></tr><tr><td>8</td><td>000336</td></tr><tr><td>4</td><td>000276</td></tr><tr><td>2</td><td>000176</td></tr></table>	<u>S.C. FREQ.</u>	<u>DATA</u>	4096	000373	2048	000353	1024	000313	512	000213	256	000375	128	000355	64	000315	32	000215	16	000356	8	000336	4	000276	2	000176
<u>S.C. FREQ.</u>	<u>DATA</u>																											
4096	000373																											
2048	000353																											
1024	000313																											
512	000213																											
256	000375																											
128	000355																											
64	000315																											
32	000215																											
16	000356																											
8	000336																											
4	000276																											
2	000176																											
2. 176142	Load Reg. 3	<table><tr><th><u>S.C. FREQ/DATA RATE</u></th><th><u>DATA</u></th></tr><tr><td>2048</td><td>174000</td></tr><tr><td>1024</td><td>176500</td></tr><tr><td>512</td><td>177000</td></tr><tr><td>256</td><td>177400</td></tr><tr><td>128</td><td>177600</td></tr><tr><td>64</td><td>177700</td></tr><tr><td>32</td><td>177740</td></tr><tr><td>16</td><td>177760</td></tr><tr><td>8</td><td>177770</td></tr><tr><td>4</td><td>177774</td></tr><tr><td>2</td><td>177776</td></tr></table>	<u>S.C. FREQ/DATA RATE</u>	<u>DATA</u>	2048	174000	1024	176500	512	177000	256	177400	128	177600	64	177700	32	177740	16	177760	8	177770	4	177774	2	177776		
<u>S.C. FREQ/DATA RATE</u>	<u>DATA</u>																											
2048	174000																											
1024	176500																											
512	177000																											
256	177400																											
128	177600																											
64	177700																											
32	177740																											
16	177760																											
8	177770																											
4	177774																											
2	177776																											
3. 176140	Load Control Reg.	002000																										
3.3.8 <u>DOD 1-13</u>																												
1. 176140	Load Control Reg.	001000																										

3.4 Output Data Definitions

- NASA 1 MSB = (16n+1) th bit after Frame Sync detected
 LSB = (16n+16) th bit after Frame Sync detected
 Where n = 0,1,2,3.....
- NASA 2 MSB = (5n+1) th bit following initialization of ONES
 LSB = (5n+5) th bit following initialization of ONES
 Where n = 0,1,2,3.....
 (First word after initialization must start with a ZERO)
- NASA 3 Frequency of Tone Burst MSB LSB
- | | | |
|------|---|------|
| 1025 | 0 | 0001 |
| 1097 | 0 | 0010 |
| 1174 | 0 | 0011 |
| 1262 | 0 | 0100 |
| 1352 | 0 | 0101 |
| 1447 | 0 | 0110 |
| 1549 | 0 | 0111 |
| 1750 | 0 | 1000 |
| 1860 | 0 | 1001 |
| 2000 | 1 | 0001 |
| 2270 | 1 | 0010 |
| 2650 | 1 | 0011 |
| 3000 | 1 | 0100 |
| 3305 | 1 | 0101 |
| 3621 | 1 | 0110 |
| 3850 | 1 | 0111 |
| 4250 | 0 | 1010 |
| 4550 | 0 | 1011 |
| 5155 | 0 | 1100 |
| 5451 | 0 | 1101 |
| 5790 | 0 | 1110 |
| 6177 | 0 | 1111 |
- NASA 4 Zero = 18 cycles = Logic 0 (CBD#0)
 One = 36 cycles = Logic 1 (CBD#1)
 Sync = 54 cycles = Transmission inhibited
- NASA 5 Lower Frequency = Logic 1 (CBD#1)
 Higher Frequency = Logic 0 (CBD#0)
- NASA 6 MSB = (16n+1) th bit after first ZERO following
 initialization of ONES
 LSB = (16n+16) th bit after first ZERO following
 initialization of ONES
 Where n = 0,1,2,3.....
- DOD 1-13 If CBD#1 = Logic ZERO, then CBD#0 = Valid Data
 (ZERO = 76 KHz, ONE = 95 KHz)
 If CBD#1 = Logic ONE, Data = SPACE (65 KHz)

3.5 Test Set Limitations

3.5.1 NASA1 and NASA6

A potential for improper data decoding of NASA 1 and NASA 6 modes exists if the phase locked oscillator fails to lock onto and distinguish from zeroes with logic ones transmitted during the initialization period. The effects of parameter variations due to temperature, voltage, aging, etc. has not been evaluated. If incorrect data detection occurs during the initialization, lack of detection of the frame sync will inhibit all word clock interrupts.

3.5.2 NASA5

Proper detection has limitations imposed by the wide range of arbitrary modulation and sub-carrier frequencies; namely:

- a. Modulation frequency range - 8Hz to 1200 Hz
- b. Sub-carrier frequency range - 7000 Hz to 21000 Hz
- c. Separation between sub-carrier frequencies corresponding to a logic 0 and 1 - Unspecified

Hardware limitations preclude the use of many filters required to extract the modulation envelope necessary for decoding the data over the wide range of allowable modulation frequencies (2 1/2 octaves). However, the use of a frequency counter and oscilloscope has verified the command encoder is generating the proper crosslink waveforms.

3.6 Test Set Demodulator Functional Breakdown

BOARD #01
(T.S. 01)

893206 (3 sheets)

Input Buffer & Conditioning Zero Crossing Generator

(N1, N3, N4, N5, N6, DOD)

Input Signal Sorting

NASA 2 Data Detection, Accumulation and Word Clock Generation

Data Bus Buffering & Control Register

BOARD #02
(T.S. 04)

893207 (3 sheets)

NASA1/NASA 6 Bit Clock Generation & Transmitted Data

Detection

NASA 1 Frame Sync Detection

Data Register #3 (Shared NASA 1 Frame Sync or NASA 6

Subcarrier/Data Rate Ratio)

Data Register #4 (Shared NASA 1 Frame Sync or NASA 5 Preset)

NASA 1/ NASA 6 Data Accumulation and Word Clock Generation

3.6 (Test Set Demodulator Functional Breakdown, Continued)

BOARD #03

(T.S. 06)

893208 (5 sheets)

Data Clock & Preset Generation (N3, N4, N5, DOD)

NASA 3 & NASA 4 Modulation Envelope Detection

NASA 3 Tone Selection and Word Clock Generation

NASA 4 Tone Selection and Word Clock Generation

NASA 5 Modulation Envelope Detection

NASA 5 Data Detection & Word Clock Generation

DOD Modulation Envelope Detection

DOD Data Detection & Word Clock Generation

Board #04

(T.S. 08)

893209 (3 sheets)

Interrupt, Address and Control Logic

Manual Test Data Interface

Output Data Sorting and Buffer Register

Data Bus Drivers

4.0 DIGITAL VOICE AND ENCRYPTER SIMULATOR MODULE

This section describes the design and implementation of the Digital Voice Generator and Encrypter Simulator module required in the Command Encoder (CE) Test Set. The Digital Voice Generator enables the uP to insert simulated digital voice in the NASA 1 output data messages, while the Encrypter Simulator serves to verify operation of the CE Encrypter Interface logic.

4.1 Digital Voice Generator, General Description

The digital voice generator enables the uP to insert simulated digital voice in the NASA 1 output messages and hence compare the received baseband demodulator output with that transmitted. The generator, shown in the functional block diagram of Figure 4-1, provides up selection from one of three fixed data patterns for serial transmission to the CE Digital Voice Interface unit.

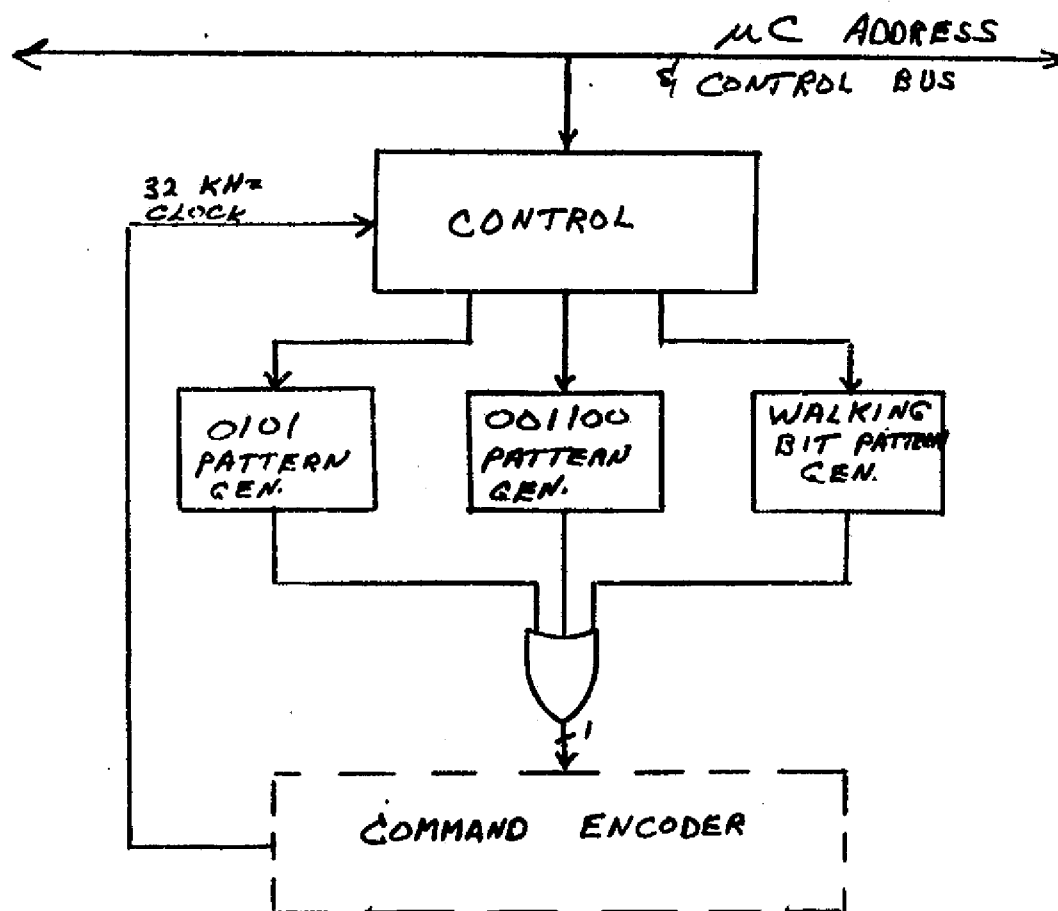


Figure 4-1

DIGITAL VOICE GEN. BLOCK DIAGRAM

4.2 Digital Voice Generator Detailed Description

The digital Voice generator provides simulated serial data patterns to the CE voice interface unit at a 32 KHz rate. Three fixed data patterns are provided; 1010 - -, 001100 - -, and a walking "1" pattern, with selection under control of the test uP.

Pattern selection is performed by issuing a uP read instruction from address 176164, 65 or 66, depending upon the pattern desired. The detailed block diagram of Figure 4-2 shows the logic referenced in the following discussion.

4.2.1 Pattern 1010 - - - and 001100 - - - Generation

A four stage counter (A) is incremented on the leading edge of each data voice clock. The first three outputs of the counter serve as address signals for two 8/1 multiplexing units. One multiplexer has inputs alternately connected in a 01010101 pattern, while the other is connected in a 00110011 pattern. Multiplexer outputs are gated by the pattern

4.2.1 (Pattern 1010 - - - and 001100 - - - Generation, Continued)

selection control logic, allowing the selected multiplexer output to be transmitted to the CE voice interface unit.

4.2.2 Walking Bit Pattern Generation

The walking bit pattern starts with a "1" in the first bit position of the first voice word to be included in the NASA 1 format with digital voice. In the second word the "1" will appear in the second bit position, and so on. Since there are eight contiguous voice words in each digital voice block of the output message, the walking bit would normally advance only to the eighth bit position and then restart at bit position one of the next block. A second walking bit has therefore been included to start at position eight and advance with each word to the sixteenth bit position.

The walking bit generator employs two 8-bit parallel input shift registers, two 1/8 demultiplexers and a 3 stage counter (B). At the start of the voice sequence, the demultiplexers address counter is initialized to zero count, resulting in a logic "1" being loaded into each shift register eight bit position. The shift registers are then shifted sixteen times with the voice clock and the output gated to the interface driver. A carryout signal is generated by counter A on the sixteenth clock pulse, incrementing counter B one count. The demultiplexer outputs are now loaded into bit position seven of each shift register, and the sequence is repeated. A timing diagram for the digital voice generator logic is shown in Figure 4-3.

4.2.3 Clear Function

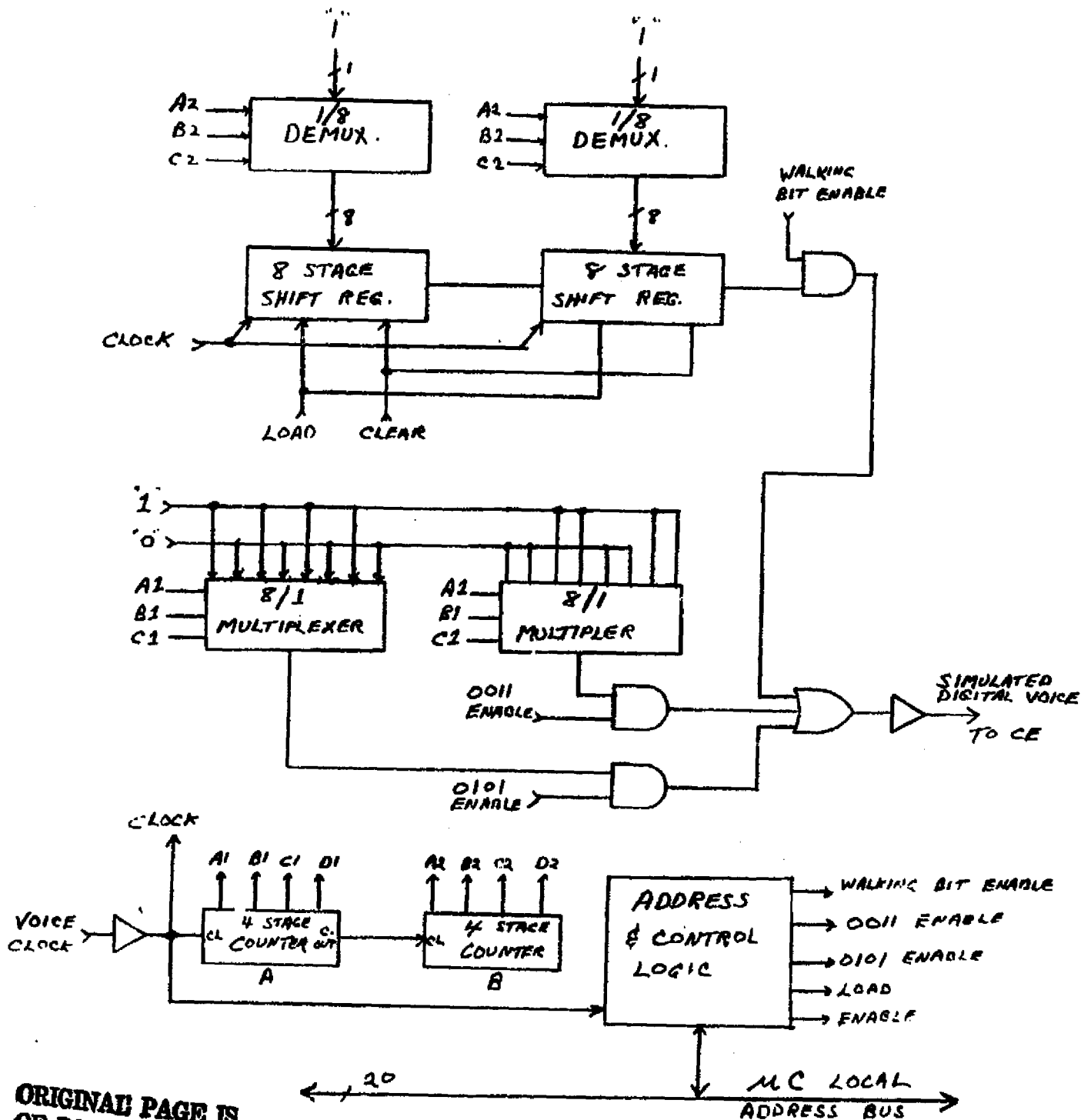
The voice generator logic can be cleared either by a programmed clear to memory address 1761667, or by the master clear control line signal (MSTCL-) activated by a local control panel switch setting.

4.2.4 Digital Voice Generator Interface

The digital voice generator interface with the CE consists of input voice clock and a serial data output port. The input clock is a 32.264 KHz \pm 0.005% square wave signal. A logic "0" = 0.0 volts \pm 0.5 volts and a Logic "1" = 5.0 volts \pm 1.0 volts. The input signal is fed into a differential line receiver, while a differential line driver transmits the serial data out. Both interface lines are twisted pairs.

4.3 Encrypter Simulator

The primary function of the encrypter simulator is to only verify the operation of the encrypter interface signals. Accordingly, the interface simply contains logic that, under control of the test set operator, either repeats or inverts the incoming data, and retransmits it back to the CE.



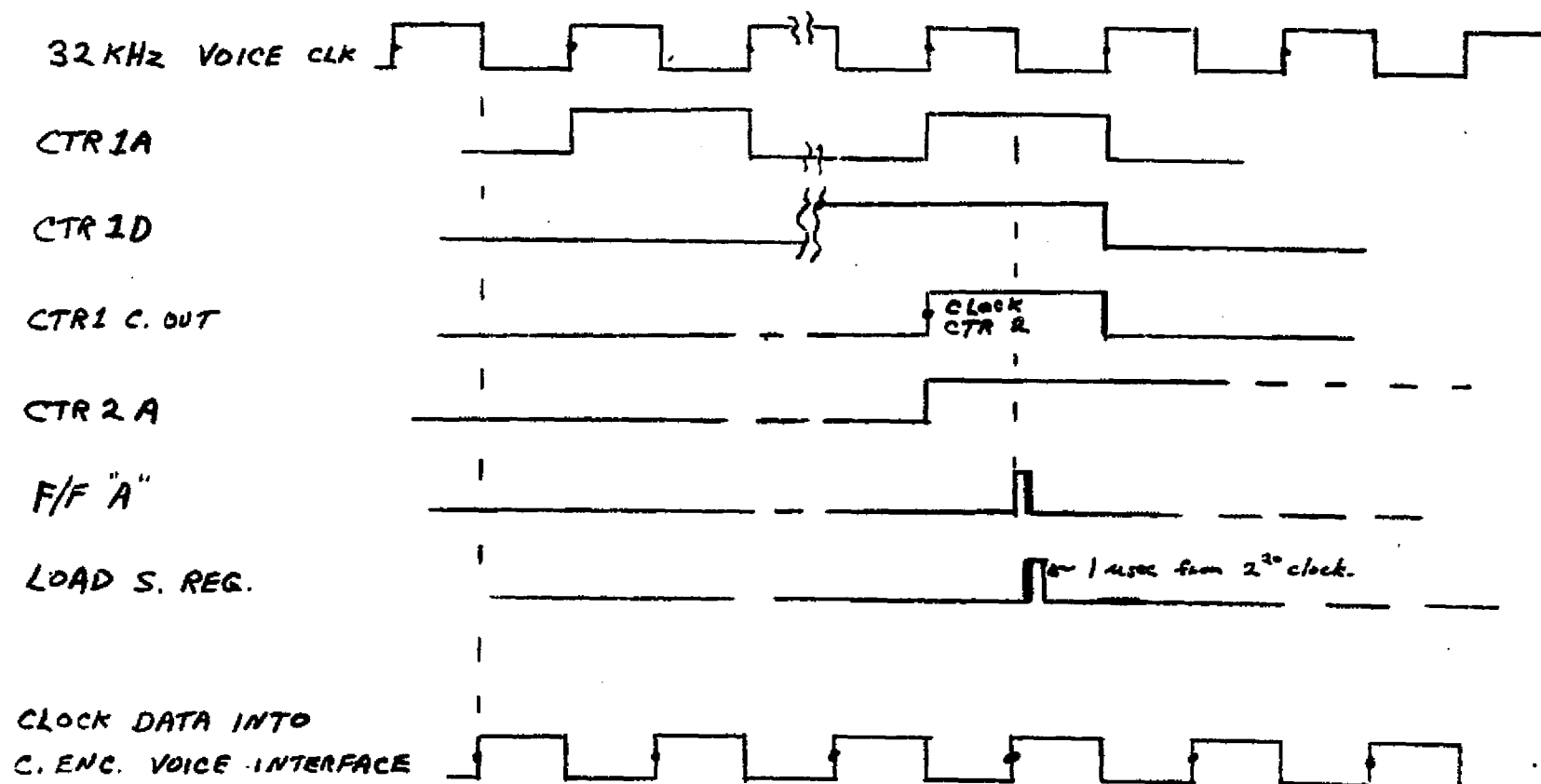


FIG 4-3 DIGITAL VOICE GENERATOR TIMING

4.3.1 Detailed Description

As shown in Figure 4-4, the leading edge of the input clock strobes the incoming data into three D-type flip-flops. If the "S" signal is a logical one, the data is returned to the CE unmodified. If the "S" signal is a zero, the "1" / "0" data is either returned or interchanged (via the 2/1 multiplexers) depending upon the state of the single bit control flip-flop set by the up.

Encrypter Simulator Interface

The input interface consists of four signals: data "1", data "0", data clock, and "S". The output interface consists of a data "1" out, data "0" out, and "S" out. Line drivers and receivers are differential, and interface cabling consists of seven twisted pairs in an overall shield.

4.4 Voice Generator and Encrypter Simulator Interface Addressing

Address decode logic is common to both units. The decode logic is activated when the upper 13 address bits are 17616X and performs a further decode on the lower 3 bits to enable the appropriate control signals. A CBACK- signal is generated in response to a correctly addressed Load or Store signal. Table 4-1 lists the function generated by each address decode. Location 176164, 176165 and 176166 are unique to the voice generator logic, while 176160 addresses only the encrypter simulator. The program clear (location 176167) is common to both functions.

Address	Function	Data Bits															
		C	H	D	1	5	-	-	-	-	-	-	-	-	-	-	C
176160	Complement Encrypter Data																
176161	Not Used																
176162	Not Used																
176163	Not Used																
176164	Enable Voice 0011 - - - Pattern																
176165	Enable Voice 0101 - - - Pattern																
176166	Enable Voice Walking Bit Pattern																
176167	Programmable Clear For Voice Generator & Encrypter Simulator																

TABLE 4-1

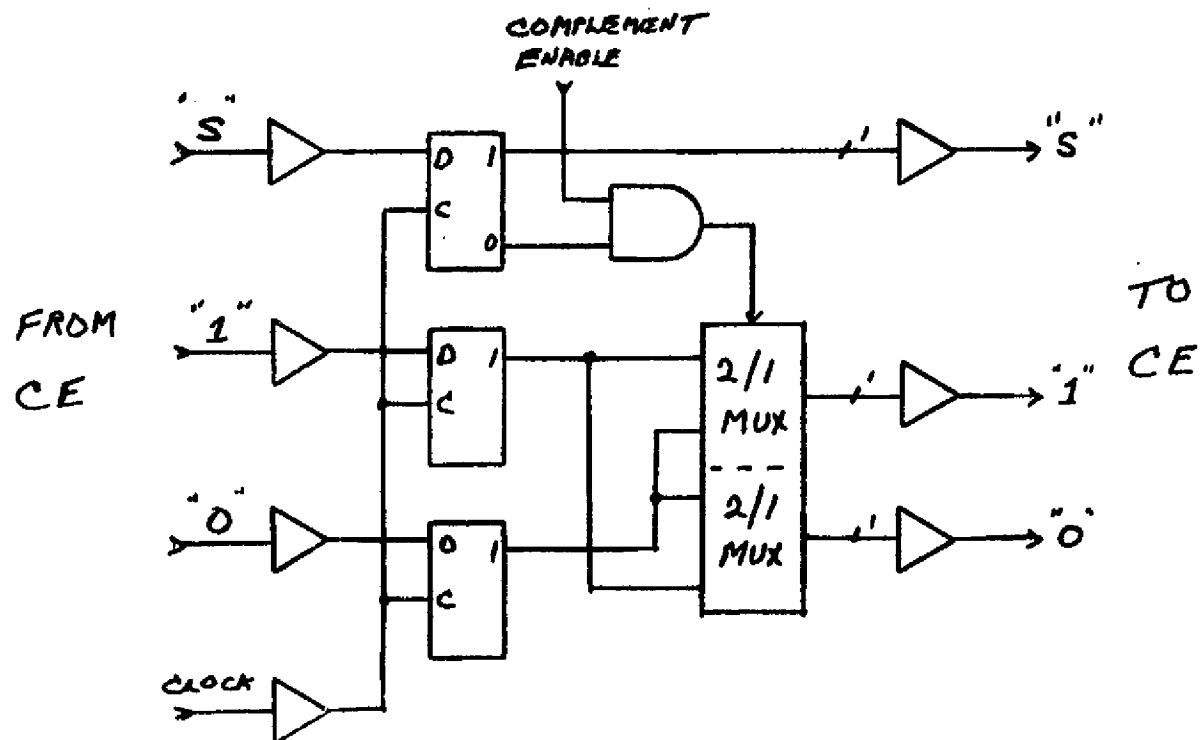


FIG. 4-4.

ENCRYPTOR SIMULATOR DETAILED BLOCK DIAG.

4.5 Detailed Logic Schematic

The detailed logic design for the voice generator and Encrypter simulator logic is shown on the two logic drawings listed below:

<u>DWG. NO.</u>	<u>SHEET #</u>	<u>LOGIC</u>
893203	1	Digital Voice Generator
	2	Encrypter Simulator and Address Logic

4.6 Miscellaneous Logic

Also located on this module are the following miscellaneous logic functions:

4.6.1 PHSI Clock Source

1 MHz PHSI clock source for the Test Set BCH Encoder, and the Hung Bus detector logic (Logic Sheet 2).

4.6.2 Hung Bus Detector

Hung Bus detection logic for the Test Set microprocessor. If a bus request (CBRQS) is not answered with a bus acknowledge (CBACK), the microprocessor would remain in a loop indefinitely. The Hung Bus detector will allow an unanswered CBRQS for about 16 usec and will then issue a CBACK. A LED on the Test Set front panel will be lit and an interrupt to the μP generated. The LED may be extinguished either by a digital voice generator and encryptor simulator clear, or by the μP bus Master Clear.

4.6.3 TTY Half-Duplex Control Logic

The current switching circuit required to implement the TTY half duplex mode of operation is located on this board (Logic Sheet 1). The voltage generated whenever a TTY key is depressed is sensed by a biased 8820 differential receiver. This receiver then drives a 75450 switching gate to interrupt the TTY input current, resulting in the corresponding TTY printout. When the TTY MODE switch S2 is in the full duplex mode (FD), the switching circuit is bypassed.

D. COMMAND ENCODER & TEST SET PACKAGING

1.0 INTRODUCTION

The Command Encoder (CE) and Command Encoder Test Set are each contained in individual cabinets containing a logic assembly and power supplies. Inter-connection between the units is via seven cables attached to the connector panels on the rear of each cabinet. A single fan in each unit provides forced air cooling. Section 2 describes the packaging approach for the Command Encoder and Test Set. Sections 3, 4 and 5 describe the module layout, inter-connections and power requirements.

2.0 PACKAGING DESCRIPTION

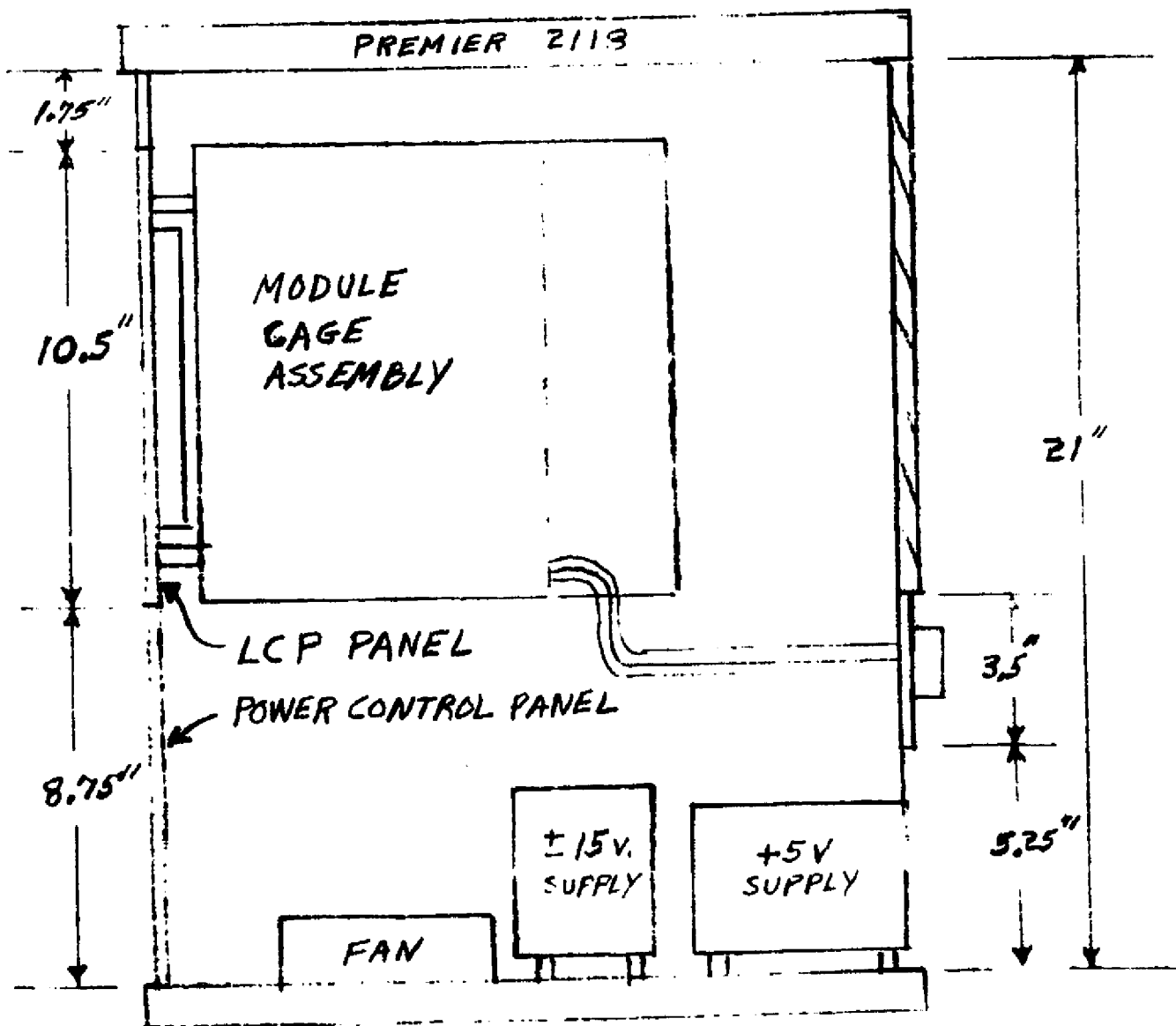
2.1 Command Encoder

The Command Encoder is housed in a Premier 2118 cabinet (see Figure 1). The module cage assembly is mounted one inch behind the Local Control Panel* on the front panel mounting flange. Three power supplies are mounted on stand-offs on the base plate toward the rear of the cabinet (see Figure 2). Convection cooling should be adequate to prevent excessive heat build up. The heated air should pass out thru the louvred rear panel and the perforated top. A fan is provided to direct air up thru the logic tray to prevent any thermal build-up in the cabinet. A power control panel is located on the front of the cabinet. This power panel (see Figure 6) contains the AC ON-OFF switch, Power on indicator, AC line fuse. Three LEDs are provided to indicate "HUNG BUS", "POWER STATUS" and "RUN". A master CLEAR switch resets the CE circuits.

2.2 Test Set

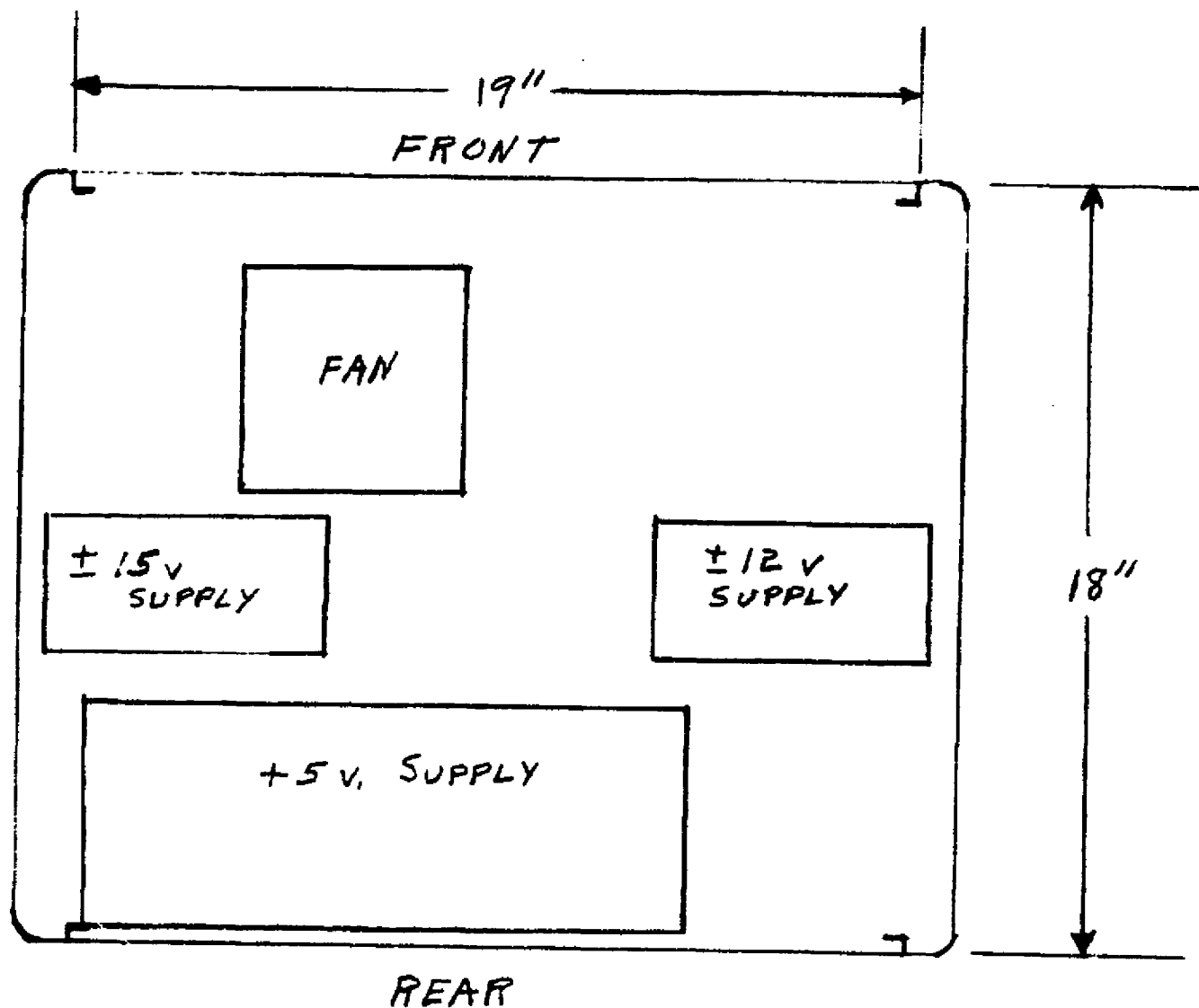
The Test Set for the Command Encoder resides in a Premier 3118 cabinet (see Figure 3). A remex RRS7300 paper tape reader is located near the top of the cabinet. The signal connections from the tape reader are hard wired to the logic tray and enter the tape reader via J1 at the rear of the same. This signal wiring is shown in Table 4. Three power supplies are mounted on stand-offs on the base plate toward the rear of the cabinet (see Figure 2) to prevent radiated heat from adversely affecting the modules in the logic cage which is mounted at the front of the cabinet 3 1/2 inches below the tape reader and 1 inch behind the Local Control Panel. A fan is mounted on the base plate below the logic tray. This fan will provide a steady stream of air directed thru the logic tray thus assisting in the removal of any heated air. The back of the cabinet is louvred and the top is perforated to allow the exit of any heated air. A power control panel (see Figure 7) is mounted below the LCP panel and contains the AC power ON/OFF switch, Power indicator and AC line fuse.

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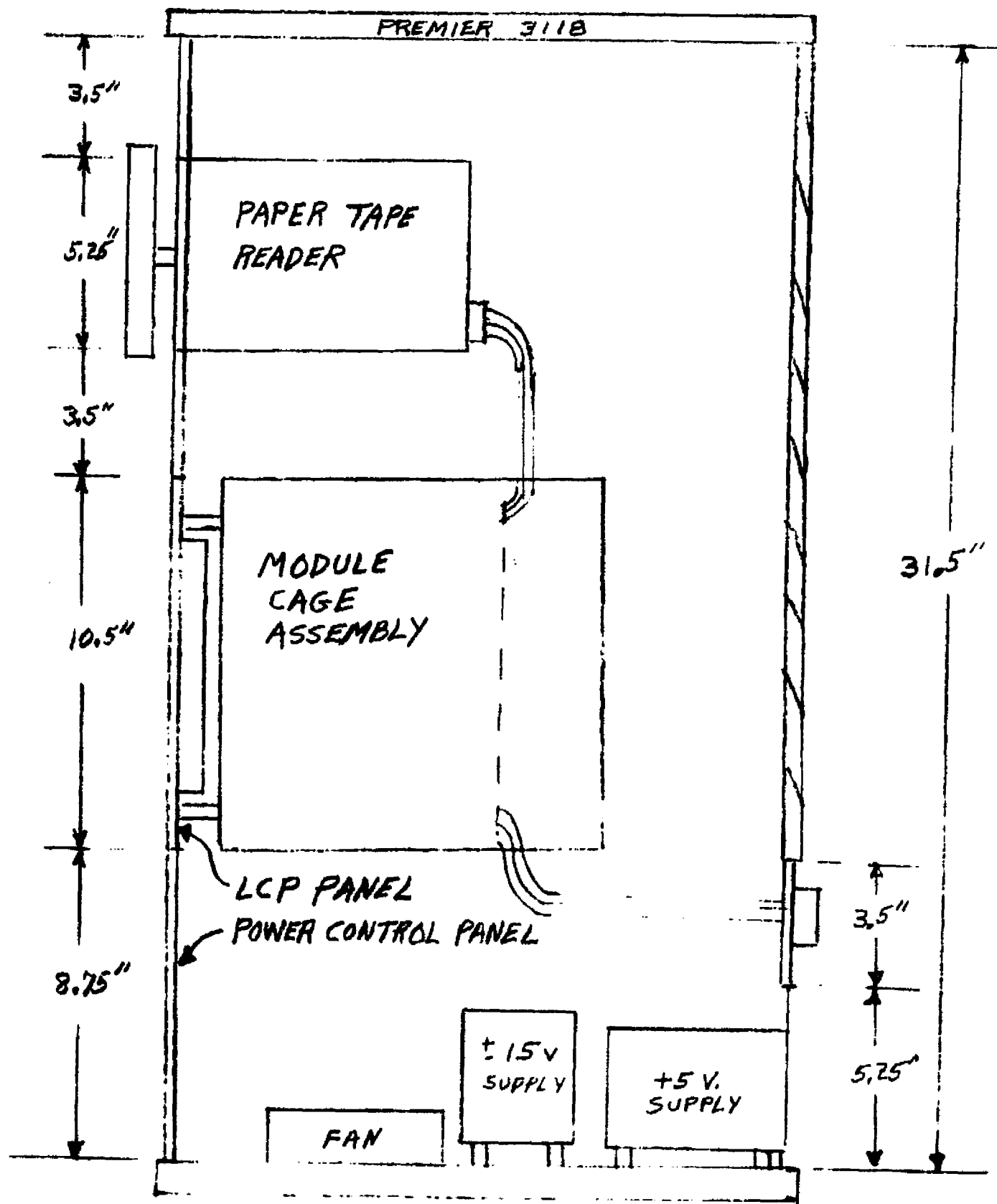
RIGHT SIDE
COMMAND ENCODER

FIG. 1



REAR
RACK BASE PLATE LAYOUT

FIG. 2



RIGHT SIDE
TEST SET

FIG. 3

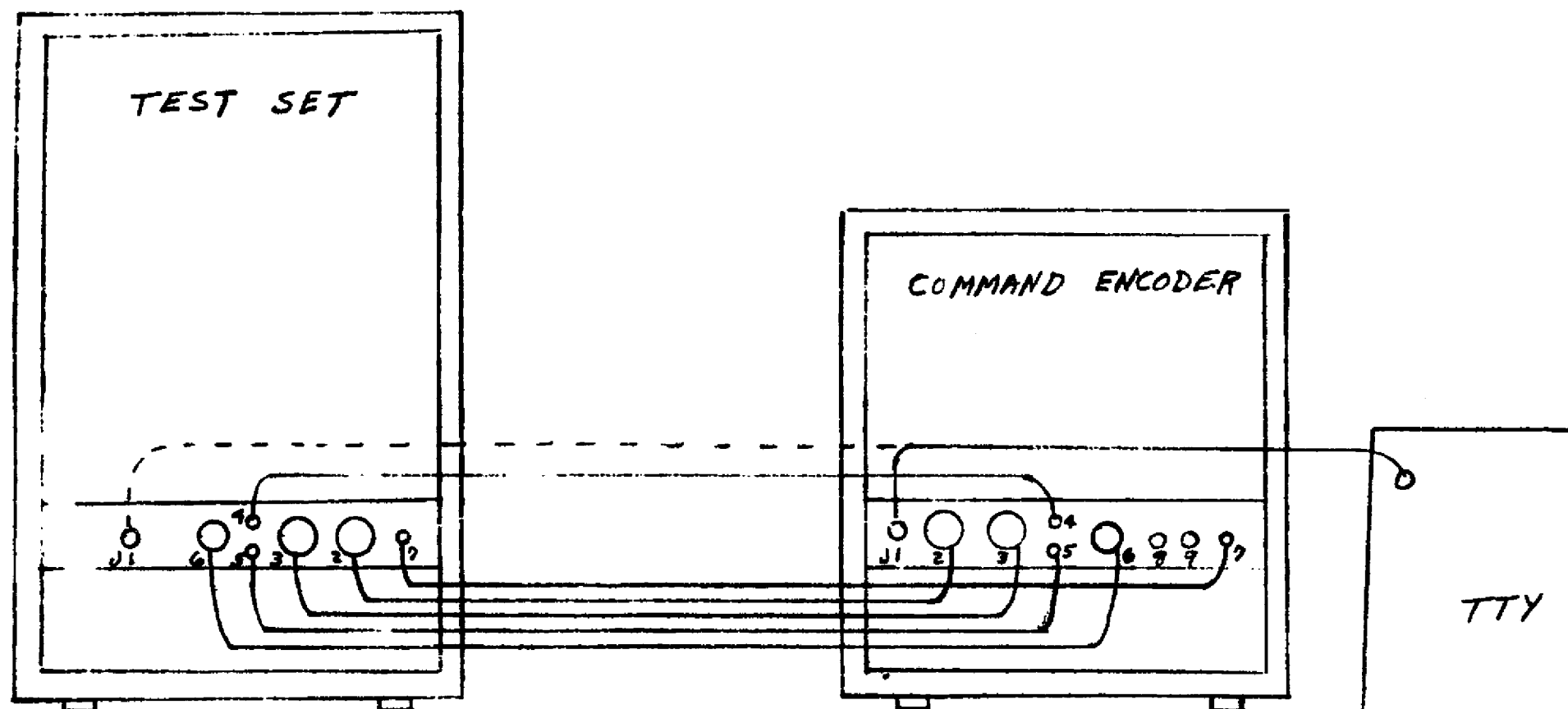
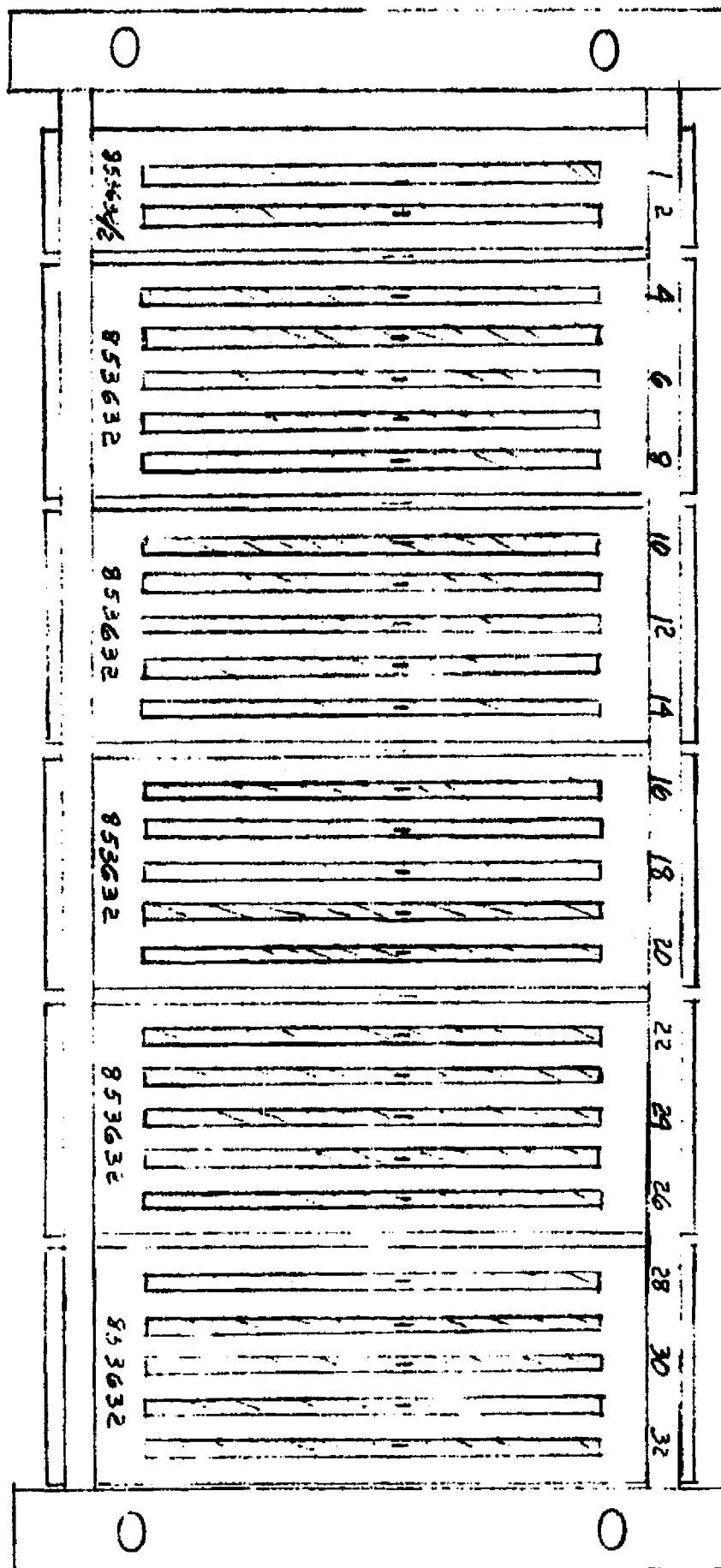


FIG. 4

REAR VIEW



☐ = Double Row
of Malco sockets

Module Side of Logic Tray

FIG 5

+5v
○
I₂

HUNG
BUS
○
I₁

PHASE
LOCK
○
I₃

AC
ON
○
OFF
SI
FI

TTY
MODE
FD
○
HD
S2

DATA
GEN
SEL
○
O
S3

MAN
CLK
GEN
○
S4

BUF
DATA
○
TP1

GND
○
TP2

CE TEST SET CONTROL PANEL

SCALE

2-172

REV

SHEET

SIZE
A

CODE IDENT NO.
49956

DRAWING NO.

FIG 6

+5V
○
I₂

HUNG
BUS
○
I₁

POWER
FAIL
○
I₃

RUN
○
I₄

AC
ON
○
OFF
SI

○
FI

MASTER
CLEAR
○
S2

CE CONTROL PANEL

SCALE	SIZE	CODE IDENT NO.	DRAWING NO.
2-173	A	49956	FIG 7
REV	SHEET		

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2.2 (Test Set, Continued)

"HUNG BUS" and "PHASE LOCK" indications are displayed by two LEDS. A two pole, two position switch permits changing the Teletype Mode from Half-Duplex to Full-Duplex. Manual clock generator and Manual data select switch are provided to aid in debug of the demodulator. "BUF DATA" may be monitored on this panel.

2.3 DC Power

Three power supplies are provided for the command encoder and for the test set. The supplies are:

- +5 Volts @ 36 Amperes Sorenson STMS-36
- +12 Volts @ 1 Ampere Sorenson PTM12-LP
- 12 Volts @ 1 Ampere Dual Supply
- +15 Volts @ .8 Ampere Sorenson PTM15-.8D
- 15 Volts @ .8 Ampere Dual Supply

The power distribution system is shown on Drawing AJM-75-5-1. In addition to the AC fuse on the power control panel, each supply has its AC power fuse.

3.0 MODULE LAYOUT

The location of the modules in the Command Encoder is shown in Table 1 which also gives the power consumption of each, as well as the DIP count.

The modules in the CE Test Set are located via Table 2. DIP count as well as power consumption is also depicted here.

3.1 Module Layout Drawings

The module layout drawings for the modulator digital and analog sections of the CE are shown in figure 8 through 12.

TABLE 1
COMMAND ENCODER MODULE LOCATION

<u>LOCATION</u>	<u>MODULE FUNCTION</u>	<u>BOARD TYPE</u>	<u>DC POWER (WATTS)</u>	<u>IC COUNT</u>	<u>DRAWING #</u>
1	Modulator Analog 1	WW	+5=.500	13	893204
2	NA		+15=3.0		
3	*		-15=3.0		
4	Modulator Analog 2	WW		8	893205
5	NA				
6	Modulator Digital 3	WW	1.102	41	893184
7	NA				

TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND
● PINS	● PINS	● PINS	● PINS	● PINS	● PINS	● PINS
TYPE VCC GND	TYPE 74L00 VCC 16 GND 7	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND	TYPE VCC GND
● PINS	● PINS 14	● PINS	● PINS	● PINS	● PINS	● PINS
TYPE 74L74 VCC 16 GND 7	TYPE 74LS193 VCC 16 GND 8	TYPE 74L75 VCC 5 GND 12	TYPE 74L00 VCC 16 GND 7	TYPE 8097 VCC 16 GND 8	TYPE 74L04 VCC 16 GND 7	TYPE VCC GND
● PINS 14	● PINS 16	● PINS 16	● PINS 14	● PINS 16	● PINS 14	● PINS
TYPE 74LS08 VCC 16 GND 7	TYPE 74LS112 VCC 16 GND 8	TYPE 74LS112 VCC 16 GND 8	TYPE 74L10 VCC 16 GND 7	TYPE 74L04 VCC 16 GND 7	TYPE 74LS05 VCC 16 GND 7	TYPE VCC GND
● PINS 14	● PINS 16	● PINS 16	● PINS 14	● PINS 14	● PINS 14	● PINS
TYPE 74L00 VCC 16 GND 7	TYPE 74L74 VCC 16 GND 7	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS112 VCC 16 GND 8
● PINS 14	● PINS 14	● PINS 16	● PINS 16	● PINS 16	● PINS 16	● PINS 16
TYPE Header VCC 7 GND 1	TYPE 7414 VCC 16 GND 7	TYPE 74L04 VCC 16 GND 7	TYPE 74LS05 VCC 16 GND 7	TYPE 74LS11 VCC 16 GND 7	TYPE 74L00 VCC 16 GND 7	TYPE 74L00 VCC 16 GND 7
● PINS 16	● PINS 14	● PINS 14	● PINS 14	● PINS 14	● PINS 14	● PINS 14
TYPE Header VCC 16 GND NA	TYPE 74L04 VCC 16 GND 7	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE VCC GND
● PINS 16	● PINS 14	● PINS 16	● PINS 16	● PINS 16	● PINS 16	● PINS
TYPE 8098 VCC 16 GND 8	TYPE 74L04 VCC 16 GND 7	TYPE 74LS138 VCC 16 GND 7	TYPE 74LS05 VCC 16 GND 7	TYPE 74L04 VCC 16 GND 7	TYPE 74L04 VCC 16 GND 7	TYPE VCC GND
● PINS 16	● PINS 14	● PINS 16	● PINS 14	● PINS 14	● PINS 14	● PINS

Figure 8
3-3-75 P.BENGTSON

TITLE: µP Interface
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A	VCC 16 GND NA	VCC 16 GND	VCC 16 GND 8	VCC 16 GND 7	VCC 16 GND 8	VCC 16 GND 8	VCC 16 GND 7
	● PINS 16	● PINS	● PINS 16	● PINS 14	● PINS 16	● PINS 16	● PINS 14
B	TYPE 74L04 VCC 16 GND 7	TYPE 74L30 VCC 16 GND 7	TYPE 74LS08 VCC 16 GND 7	TYPE VCC GND	TYPE 74LS10 VCC 16 GND 7	TYPE 74L30 VCC 16 GND 7	TYPE 74L04 VCC 16 GND 7
	● PINS 14	● PINS 14	● PINS 14	● PINS	● PINS 14	● PINS 14	● PINS 14
C	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8	TYPE 74L74 VCC 16 GND 7	TYPE 74LS11 VCC 16 GND 7	TYPE 74LS00 VCC 16 GND 7	TYPE 74LS193 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8
	● PINS 16	● PINS 16	● PINS 14	● PINS 14	● PINS 14	● PINS 16	● PINS
D	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE 74L30 VCC 16 GND 7	TYPE 74LS112 VCC 16 GND 8	TYPE 74LS112 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8
	● PINS 16	● PINS 16	● PINS 14	● PINS 16	● PINS 16	● PINS 16	● PINS 16
E	TYPE 74LS08 VCC 16 GND 7	TYPE 74LS08 VCC 16 GND 7	TYPE 74LS112 VCC 16 GND 8	TYPE 74LS86 VCC 16 GND 7	TYPE 8098 VCC 16 GND 8	TYPE 74LS08 VCC 16 GND 7	TYPE 74LS08 VCC 16 GND 7
	● PINS 14	● PINS 14	● PINS 16	● PINS 14	● PINS 16	● PINS 14	● PINS 14
F	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8	TYPE 74L00 VCC 16 GND 7	TYPE 74LS86 VCC 16 GND 7	TYPE 74LS86 VCC 16 GND 7	TYPE 74LS175 VCC 16 GND 8	TYPE 74LS175 VCC 16 GND 8
	● PINS 16	● PINS 16	● PINS 14	● PINS 14	● PINS 14	● PINS 16	● PINS 16
G	TYPE 74LS83 VCC 5 GND 12	TYPE 74LS83 VCC 5 GND 12	TYPE 74LS17 VCC 16 GND 8	TYPE 82S129 VCC 16 GND 8	TYPE 82S129 VCC 16 GND 8	TYPE 74LS83 VCC 5 GND 12	TYPE 74LS83 VCC 5 GND 12
	● PINS 16	● PINS 16	● PINS 16	● PINS 16	● PINS 16	● PINS 16	● PINS 16
H	TYPE 74L95 VCC 4 GND 13	TYPE 74L95 VCC 4 GND 13	TYPE 74LS17 VCC 16 GND 8	TYPE 74LS193 VCC 16 GND 8	TYPE 8098 VCC 16 GND 8	TYPE 74L95 VCC 4 GND 13	TYPE 74L95 VCC 4 GND 13
	● PINS 14	● PINS 14	● PINS 16	● PINS 16	● PINS 16	● PINS 14	● PINS 14
	1	2	3	4	5	6	7

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112

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TYPE 74 Modulator
SERIAL NO. 84233

Figure 9

A	TYPE VCC GND ③ PINS	TYPE 74LS175 VCC 16 GND 8 ③ PINS 16	TYPE 74LS175 VCC 16 GND 8 ③ PINS 16	TYPE VCC GND ③ PINS	TYPE VCC GND ③ PINS	TYPE VCC GND ③ PINS	TYPE VCC GND ③ PINS
	TYPE VCC GND ③ PINS	TYPE 825129 VCC 16 GND 8 ③ PINS 16	TYPE 825129 VCC 16 GND 8 ③ PINS 16	TYPE 898-1-K VCC 16 GND NA ③ PINS 16	TYPE VCC GND ③ PINS	TYPE VCC GND ③ PINS	TYPE VCC GND ③ PINS
	TYPE VCC GND ③ PINS	TYPE 74LS10 VCC 16 GND 7 ③ PINS 14	TYPE 74LS86 VCC 16 GND 7 ③ PINS 14	TYPE 8098 VCC 16 GND 8 ③ PINS 16	TYPE 74LS74 VCC 16 GND 7 ③ PINS 14	TYPE 74LS00 VCC 16 GND 7 ③ PINS 14	TYPE VCC GND ③ PINS
	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14
	TYPE 74LS174 VCC 16 GND 8 ③ PINS 16	TYPE 74LS08 VCC 16 GND 7 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS74 VCC 16 GND 7 ③ PINS 14	TYPE 74LS174 VCC 16 GND 8 ③ PINS 16	TYPE 74LS174 VCC 16 GND 8 ③ PINS 16
	TYPE 74LS83 VCC 5 GND 12 ③ PINS 16	TYPE 74LS83 VCC 5 GND 12 ③ PINS 16	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS83 VCC 5 GND 12 ③ PINS 16	TYPE 74LS83 VCC 5 GND 12 ③ PINS 16	TYPE 74LS83 VCC 5 GND 12 ③ PINS 16
	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS74 VCC 16 GND 7 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14
	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 825129 VCC 16 GND 8 ③ PINS 16	TYPE 825129 VCC 16 GND 8 ③ PINS 16	TYPE 8098 VCC 16 GND 8 ③ PINS 16	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14	TYPE 74LS95 VCC 4 GND 13 ③ PINS 14

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Figure 10
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SUB-CORP. 893184

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TYPE VCC GND 14 ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND R1 R2 ① PINS	TYPE VCC GND R14 R31 ① PINS	TYPE VCC GND R32 R33 ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS
TYPE DAC VCC 372WB GND A1-14 ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE V/F VCC GND ① PINS
TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE COMP VCC GND 8 ① PINS 16	TYPE DG151 VCC GND 12 ① PINS 14	TYPE COMP VCC GND 10 ① PINS 16	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS
TYPE VCC GND 11-14 ① PINS	TYPE VCC GND ① PINS	TYPE COMP VCC GND 8 ① PINS 16	TYPE DG151 VCC GND 12 ① PINS 14	TYPE COMP VCC GND 8 ① PINS 16	TYPE VCC GND ① PINS	TYPE VCC GND 16 ① PINS
TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE COMP VCC GND 12 ① PINS	TYPE 318D VCC GND ① PINS 14	TYPE MC1594 VCC GND 3 ① PINS 16	TYPE COMP VCC GND 8 ① PINS 16	TYPE VCC GND R16 ① PINS
TYPE DAC VCC 372WB GND D1-14 ① PINS	TYPE VCC GND ① PINS	TYPE COMP VCC 16 GND 8 ① PINS 16	TYPE COMP VCC GND 1 ① PINS 16	TYPE 318D VCC GND ① PINS 14	TYPE 7403 VCC 16 GND 7 ① PINS 14	TYPE VCC GND R15 ① PINS
TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE VCC GND ① PINS	TYPE 318D VCC GND ① PINS 14	TYPE COMP VCC GND 4 ① PINS 16	TYPE COMP VCC 1 GND 7 ① PINS 16	TYPE COMP VCC GND 13 ① PINS 16
TYPE 74L95 VCC 4 GND 13 ① PINS 14	TYPE 74L95 VCC 4 GND 13 ① PINS 14	TYPE CO338E VCC 16 GND 7 ① PINS 14	TYPE COMP VCC GND 3 ① PINS 16	TYPE VCC GND ① PINS	TYPE COMP VCC GND 9 ① PINS 16	TYPE COMP VCC GND 1 ① PINS 16

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FIG. 11

TITLE: MODULATOR, ANALOG NO. 1

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A	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS
B	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS
C	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE COMP VCC — GND 8 ② PINS 16	TYPE COMP VCC — GND 3 ② PINS 16	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS
D	TYPE COMP VCC — GND — ② PINS 16	TYPE COMP VCC — GND — ② PINS 16	TYPE COMP VCC 11 GND 15 ② PINS 16	TYPE COMP VCC — GND 9 ② PINS 16	TYPE COMP VCC — GND 9 ② PINS 16	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS
E	TYPE COMP VCC 3 GND — ② PINS 16	TYPE 74123N VCC 16 GND 8 ② PINS 16	TYPE 361D VCC 16 GND 12 ② PINS 14	TYPE 361D VCC 16 GND 12 ② PINS 14	TYPE 318D VCC — GND — ② PINS 14	TYPE 318D VCC — GND — ② PINS 14	TYPE VCC GND ② PINS
F	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE 74LOON VCC 16 GND 7 ② PINS 14	TYPE 74LOON VCC 16 GND 7 ② PINS 14	TYPE 7403N VCC 16 GND 7 ② PINS 14	TYPE COMP VCC — GND 10 ② PINS 16	TYPE VCC GND ② PINS
G	TYPE VCC GND ② PINS	TYPE VCC GND ② PINS	TYPE COMP VCC 14 GND 9 ② PINS 16	TYPE COMP VCC — GND 8 ② PINS 16	TYPE COMP VCC — GND — ② PINS 16	TYPE 318D VCC — GND — ② PINS 14	TYPE COMP VCC — GND 1 ② PINS 16
H	TYPE VCC GND ② PINS	TYPE 7407N VCC 16 GND 7 ② PINS 14	TYPE DG151BP VCC — GND — ② PINS 14	TYPE DG151BP VCC — GND — ② PINS 14	TYPE DG151BP VCC — GND — ② PINS 14	TYPE COMP VCC — GND 8 ② PINS 16	TYPE COMP VCC — GND 14 ② PINS 14

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 TITLE: CE 04 MOD. ANALOG NO. 2 FIG 12
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 2-179

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<u>LOCATION</u>	<u>MODULE FUNCTION</u>	<u>BOARD TYPE</u>	<u>DC POWER (WATTS)</u>	<u>IC COUNT</u>	<u>DRAWING #</u>
8	Modulator Digital 2	WW	1.273	52	893183
9	*				
10	Modulator Digital 1	WW	.530	36	893185
11	NA				
12	Tape Reader (prewired)***	WW			853862
13	NA				
14	VOICE/ENCRYPTER I/F	WW	2.18	36	893202
15	*				
16	BCH	WW	1.58	42	893201
17	NA				
18	FUTURE SPARE (MIA A)	WW			
19	NA				
20	FUTURE SPARE (MIA B)	WW			
21	*				
22	FUTURE SPARE (INPUT HANDLER)	WW			
23	TERMINATOR MODULE	PC		893216	
24	4KX16 2 PORT MEM	PC	13.3	48	853581
25	1KX16 2 PORT MEM	PC	13.1	48	893217
26	PIN (Priority Int. Net)	PC	5.0	37	853868
27	*				
28	ALCM (TTY Interface) ***	PC	5.0	45	853834
29	2KX16 RAM (prewired)	PC			
30	AU (Arithmetic Unit)	PC		47	851702
31	CU (Control Unit)	PC	25.0	48	853545
32	LCP (Control Panel)**	PC	7.0	37	**893214 or 853679

WW = Wire Wrap board

* = No Malco Socket

NA = Space occupied by adjacent module

PC = Printed Circuit Board

** = Replaced by LCP Jumper card when Command Encoder is under control of Test Set.

All power for +5 volts except as noted.

*** = Not Used

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TABLE 2
CE TEST SET MODULE LOCATION

<u>LOCATION</u>	<u>MODULE FUNCTION</u>	<u>BOARD TYPE</u>	<u>DC POWER (WATTS)</u>	<u>IC COUNT</u>	<u>DRAWING #</u>
1	Demodulator 1	WW		30	893206
2	NA				
3	*				
4	Demodulator 2	WW		46	893207
5	NA		+5=45.0		
6	Demodulator 3	WW	+15=3.0 -15=3.0	44	893208
7	NA				
8	Demodulator 4	WW		35	893209
9	*				
10	(Connector tie points)	WW	NA	NA	
11	NA				
12	VOICE/ENCRYPTER SIM.	WW	4.2	39	893203
13	NA				
14	BCH ENCODER	WW	1.58	42	893201
15	*				
16	SPARE	WW			
17	NA				
18	FUTURE SPARE (MIA A)	WW			
19	NA				
20	FUTURE SPARE (MIA B)	WW			
21	*				
22	SPARE	WW			
23	TAPE READER I/F	PC	5.0	43	853862
24	SPARE	PC			
25	4KX16 2 PORT MEM (RAM)	PC	7.7	48	853581
26	PIN	PC	5.0	37	853868
27	*				
28	ALCM	PC	5.0	45	853834

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<u>LOCATION</u>	<u>MODULE FUNCTION</u>	<u>BOARD TYPE</u>	<u>DC POWER (WATTS)</u>	<u>IC COUNT</u>	<u>DRAWING #</u>
29	2KX16 MEM (RAM)	PC	TBD	TBD	851707
30	AU	PC		47	851702
31	CU	PC	25	48	853545
32	LCP	PC	7	37	853679

WW = Wire Wrap board

* = No Malco Socket

NA = Space occupied by adjacent module

PC = Printed Circuit Board

All power for +5 Volts unless otherwise noted.

4.0 DEVICE TECHNOLOGY

Table 3 lists the technology used for the majority of the logic for each unit in the CE and Test Set.

TABLE 3

<u>Unit</u>	<u>Logic Type</u>
CE Microprocessor	Standard TTL
CE Modulator - Digital	Low Power TTL
CE BCH Encoder	Low Power TTL
CE Voice/Encryptor Interface	Low Power TTL
CE 1K Memory	Schottky and Std. TTL
CE 4K Memory	MOS
Test Set Microprocessor	Standard TTL
Test Set Demodulator	Standard TTL
Test Set BCH Encoder	Low Power TTL
Test Set Voice/Encryptor Sim.	Low Power TTL
Test Set 2K RAM	MOS
Test Set 4K RAM	MOS

5.0 SIGNAL INTERCONNECTION

Signals between the Command Encoder and the CE Test Set will be transferred via cables attached to connectors on 3 1/2 panels at the rear of each unit (see Figure 4). The signal allocation for each connector is shown in Tables 4 & 5. Note that the Teletypewriter may be connected to either cabinet via J1 on the connector panel. The internal wires from the connectors are wire-wrapped to the logic tray. All signals are transferred by either twisted pair or coaxial cable.

J2-A	CBD00-	J2-b	CBD12-
-B	CBD00-RET	-c	CBD12-RET
-C	CBD01-	-d	CBD13-
-D	CBD01-RET	-e	CBD13-RET
-E	CBD02-	-f	CBD14-
-F	CBD02-RET	-g	CBD14-RET
-G	CBD03-	-h	CBD15-
-H	CBD03-RET	-i	CBD15-RET
-J	CBD04-	-j	
-K	CBD04-RET	-k	
-L	CBD05-	-m	CBRQS-
-M	CBD05-RET	-n	* CBRQS-RET
-N	CBD06-	-p	Shield
-P	CBD06-RET	-q	CBACK-
-R	CBD07-	-r	CBACK-RET
-S	CBD07-RET	-s	MSTCL-
-T	CBD08-	-t	MSTCL-RET
-U	CBD08-RET	-u	CBWRT-
-V	CBD09-	-v	CBWRT-RET
-W	CBD09-RET	-w	
-X	CBD10-	-x	
-Y	CBD10-RET	-z	
-Z	CBD11-	-AA	
J2-Q	CBD11-RET	J2-PP	

TABLE 4A

* Shielded twisted pair

J3 - A	CBA00 -	J3 - b	CBA12 -
- B	CBA00 - RET	- c	CBA12 - RET
- C	CBA01 -	- d	CBA13 -
- D	CBA01 - RET	- e	CBA13 - RET
- E	CBA02 -	- f	CBA14 -
- F	CBA02 - RET	- g	CBA14 - RET
- G	CBA03 -	- h	CBA15 -
- H	CBA03 - RET	- i	CBA15 - RET
- J	CBA04 -	- j	
- K	CBA04 - RET	- k	
- L	CBA05 -	- m	
- M	CBA05 - RET	- n	
- N	CBA06 -	- p	
- P	CBA06 - RET	- r	
- R	CBA07 -	- s	
- S	CBA07 - RET	- t	
- T	CBA08 -	- u	
- U	CBA08 - RET	- v	
- V	CBA09 -	- w	
- W	CBA09 - RET	- x	
- X	CBA10 -	- y	
- Y	CBA10 - RET	- z	
- Z	CBA11 -	- AA	
J3 - a	CBA11 - RET	J3 - BB	

TABLE 4 B

J6 - 1	ENCR S OUT +	J1 - A
- 2	ENCR S OUT -	- B
- 3	ENCR 1 OUT +	- C TTIN +
- 4	ENCR 1 OUT -	- D TTIN -
- 5	ENCR 0 OUT +	- E TTOUT -
- 6	ENCR 0 OUT -	- F TTOUT +
- 7	ENCR S IN +	J1 - H
- 8	ENCR S IN -	
- 9	ENCR 1 IN +	
- 10	ENCR 1 IN -	J4 - IN VOICE DATA +
- 11	ENCR 0 IN +	J4 - OUT VOICE DATA -
- 12	ENCR 0 IN -	
- 13	ENCR CLK IN +	J5 - IN VOICE CLK +
- 14	ENCR CLK IN -	J5 - OUT VOICE CLK -
- 15		
- 16		J7 - IN CROSS LINK
- 17		J7 - OUT CROSS LINK RET
- 18		
- 19		J8 - IN LOAD SYNC
- 20		J8 - OUT LOAD SYNC RET
- 21		
- 22		J9 - GND
- 23		
J6 - 24		

TABLE 4 C

INTERCONNECTIONS FOR TAPE READER

SYSTEM NOMENCLATURE	From TEST SET	To TAPE READER	READER NOMENCLATURE
RDO- GND 0,1,2 } TP	23-109 23-110	J1-1 J1-11	CH1 OUT OV
RD1- GND 0,1,2 } TP	23-107 23-110	J1-2 J1-11	CH2 OUT OV
RDE- GND 0,1,2 } TP	23-106 23-110	J1-3 J1-11	CH3 OUT OV
RD3- GND 3,4 } TP	23-105 23-108	J1-4 J1-12	CH4 OUT OV
RD4- GND 3,4 } TP	23-103 23-108	J1-5 J1-12	CH5 OUT OV
RD5- GND 5,6,7 } TP	23-101 23-102	J1-6 J1-13	CH6 OUT OV
RD6- GND 5,6,7 } TP	23-100 23-102	J1-7 J1-13	CH7 OUT OV
RD7- GND 5,6,7 } TP	23-99 23-102	J1-8 J1-13	CH8 OUT OV
RDSTRB- GND PR } TP	23-97 23-98	J1-9 J1-24	DATRDY OUT OV
RC1 DRIVE CONTROL GND } TP	23-93 23-98	J1-16 J1-24	DRIVE RIGHT OV
RC2 DRIVE CONTROL GND } TP	23-95 23-98	J1-17 J1-24	DRIVE LEFT OV
READER STATUS- GND } TP	23-96 23-98	J1-14 J1-24	SYS RDY OV

TABLE 5.

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III. COMMAND ENCODER SOFTWARE

1.0 SOFTWARE REQUIREMENTS/PERFORMANCE

Inputs to the CE are received from three logical sources: (a) Command Channel, for processing instructions and commands; (b) Performance Monitor System (PMS) Channel, for validation data feedback; (c) digital voice input. Inputs (a) and (b) are through the two-port RAM (presumably via the Input Interface Unit or the Test Set). Status information is generated for both (a) and (b) and is available via the two-port RAM.

The Coding and Format Generation unit accepts 19 different types (6NASA and 13DOD) of commands, formats them, encodes them, and drives the programmable modulator. In addition, NASA1 commands may be time multiplexed with digital voice data. All DOD commands are passed through the encrypter interface. A transparent data mode is accepted in all command types, except NASA3 and NASA4.

The Coding and Format Generation unit also accepts validation data from the PMS channel and performs the requested validations and retransmission as necessary.

1.1 Functional Operation

The overall functional operation of the CE is depicted in Figure 1.1. As can be seen from the flow diagram, once the presence of a new command is detected, the Auxiliary Computer first reads the memory location in the CE containing the status word (CCSW). If the Command Instruction (CI) request bit and the Data Block (DB) request bit are set, the computer writes appropriate information into the instruction, data block and Command Channel Message (CCMSG) locations of the CE's input memory. Receipt of the CCMSG precipitates an Input Interrupt which initiates the processing of the new command by the Coding and Format Generation Unit (CFG). This unit buffers the input data block and updates the CCSW to indicate that a new DB can be transmitted. The command instruction is decoded, and the modulator unit is set to start the initialization sequence. The modulator's data request interrupt is serviced until a command word is completed, at which time the interval timer is set for 30 ms (validation response overdue time).

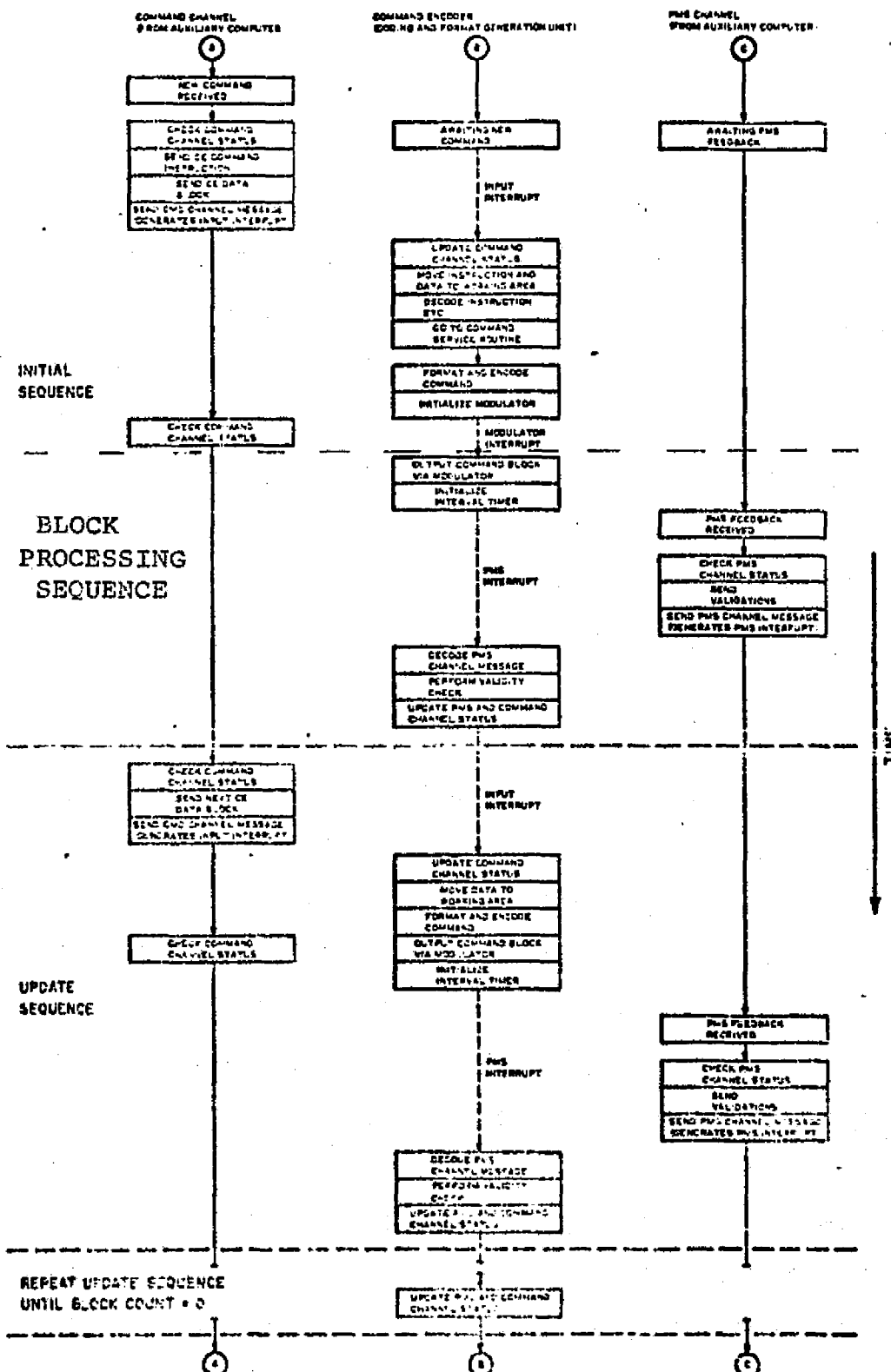


Figure 1-1 Command Encoder Overall Operational Flow Diagram

When the auxiliary computer detects the presence of validation data, it checks the Performance Monitor System Channel Status Word (PMSSW), transfers data to the appropriate input memory buffer, and issues a PMS Channel Message (PMSMSG). Receipt of the PMSMSG generates the PMS Interrupt causing the CE to perform the requested validity checks and update the PMSSW.

The above sequence is repeated for each command word until the DB is complete. The cycle is resumed with the next DB and continues until the last DB is complete.

The presence of higher priority commands within the Auxiliary Computer requires the issuance of a "HIPRI" CCMMSG to effect an orderly abortion of the command presently in progress.

1.2 Data Terminology

The Command Instruction specifies a FILE of data to be processed by the Command Encoder. The file is composed of up to 511 DATA BLOCKS. Each block consists of 1 to 16 RECORDS. Each record starts on a RP-16 WORD boundary and is composed as dictated by the particular format type (64 bit max.). Each input record is transformed by the Coding and Format Generation Unit into an output record composed as dictated by the format type (160 bit max.).

1.3 Buffering

Command channel input (CI and DB) is double buffered. To effect the buffering within a reasonable time, a buffer swapping approach is used. This adds complexity to the Input Interface Unit but expands the range of addressable locations from 511 to the entire CE memory.

The original Auxiliary Computer to Input Interface unit message formats are summarized in Figure 1.2. The CE MEMORY ADDRESS field specified an address in the CE memory which was to be the starting address for the requested transfer. The specified address will, instead, contain the starting address. That is, all I/O by the Input Interface unit to the two-port RAM will be indirect.

The Command Encoder I/O buffer memory map is shown in Figure 1.3.

COMMAND WORD FORMAT

1	3 4	8 9	13 14	22 23	27 28
CMD SYNC	CE ADDRESS	MODE CONTROL FIELD	CE MEMORY ADDRESS	BLOCK LENGTH	PARITY

COMMAND DATA WORD FORMAT

1	3 4	8 9	24 25	26	27	28
DATA SYNC	CE ADDRESS	DATA	PATTERN CHECK			PARITY
			1	0	1	

RESPONSE DATA WORD FORMAT

1	3 4	8 9	24 25	26	27	28
DATA SYNC	CE ADDRESS	DATA	PWR STATUS	-	VAL BITE	PARITY

Figure 2-3. Summary of Message Formats

1 Command Word (CW)

The Command Word will contain the following information:

Bits	Field Description
1 - 3	<u>Command Sync</u> - Three-bit code for a Command Word Sync.
3 - 8	<u>CE Address</u> - Five-bit code which identifies that the CE must respond to the transmitted Command Word.
9 - 13	<u>Mode Control Field</u> - Five-bit code used for determining the operational mode of the CE as follows: <ul style="list-style-type: none"> 9 - Return Received Command Data Word 10 - Send BITE Status 11 - Master Reset 12 - Transmit/Receive 13 - Address - Identifies when CE Memory Address specifies input/output buffer memory location or the external control register within the Coding and Format Generation Unit.

Bits

Field Description

- 14 - 22 CE Memory Address - Nine-bit code that identifies the address of the command encoder memory location. This code also identifies a starting address for a multiple-word data transfer.
- 23 - 27 Block Length - Five-bit code that identifies the number of data words to be transmitted or received. For a non-zero code, the CE will transmit/receive words from/to monotonically increasing addresses starting at the specified CE memory address.
- 28 Parity - Odd Parity.

2 Command Data Word (CDW)

The Command Data Word will contain the following information:

Bits

Field Description

- 1 - 3 Data Sync - Three-bit code for a Command Data Word sync.
- 4 - 8 CE Address - Five-bit code which identifies that CE must accept the transmitted Command Data Word.
- 9 - 24 Data - Contains the data to be transferred into the CE.
- 25 - 27 Pattern code for message validity test.
- 28 Parity - Odd parity.

3 Response Data Word (RDW)

The Response Data Word will contain the following information:

Bits

Field Description

- 1 - 3 Data Sync - Three-bit code for a Response Data Word sync.
- 4 - 8 CE Address - Five-bit code which identifies that the CE is responding to the Command Word.
- 9 - 24 Data - Contains the requested data.
- 25 Power Status - Indicates the occurrence of a CE power down/power up sequence since the transmission of the last message.
- 26 Unused
- 27 Validity (BITE) - Indicates the status of the CE.
- 28 Parity - Odd parity.

Figure 1 - 2

Auxiliary Computer - Input Interface Unit

ssa Fo ts

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<div>← 16b →</div>		
0	Reserved for Initialization and HIRPI Interrupt	
1	CCSW POINTER	
2	CURRENT CI INPUT BUFFER POINTER	
3	CURRENT DB (1-32) BUFFER POINTER	
4	CURRENT DB (33-64) BUFFER POINTER	
5	CCMSG POINTER	
6	PMSSW POINTER	
7	ECHO BUFFER POINTER	
10	BIT-BY-BIT BUFFER POINTER	
11	PMSMSG POINTER	
12	POINTER TO NEXT LOCATION	
13	RESERVED FOR DEBUG	
14	BITE STATUS WORD POINTER	
15	ERONEOUS CCMSG WORD POINTER	
16	ERONEOUS PMSMSG WORD POINTER	
	COMMAND INSTRUCTION INPUT BUFFER	4 WORDS
	COMMAND INSTRUCTION WORKING BUFFER	9 WORDS
	DB BUFFER (1)	64 WORDS
	DB BUFFER (2)	64 WORDS
	ECHO BUFFER	10 WORDS
	BIT BY BIT BUTFER	10 WORDS

FIGURE 1-3
CE I/O BUFFER MEMORY MAP

1.4 Formatting

Output Record Formats for the 6 NASA types and the 13 DOD types is specified in Section II, A2.5. Transparent mode (i.e., no formatting or encoding) leads to new definitions of some types of input records. These are specified in 4.4 of this section.

1.5 Validations

Bit-by-bit and Echo validations will be done on an output record basis. It is assumed that PMS data will be returned in Output Record Formats. No validations will be done in transparent mode.

2.0 BLOCK DESCRIPTION

Figure 2.1 depicts a block diagram of the logical breakdown of CE software functions.

2.1 Command Channel Interface

Intercepts Command Channel interrupts, decodes the Command Channel Message, updates the Command Channel Status Word (CCSW), and signals the appropriate action.

2.2 Output Format Generation Module

Performs all Command Channel handshaking, instruction decoding, and command formatting (see Figure 2.2 for detailed block diagram). It also starts the modulator.

2.3 Modulator Driver/Validation Control (MDVC)

Accepts a record from the Output Format Generator and passes it to the modulator data interrupt handlers. It times the validation response and initiates retransmission on validation failures.

2.4 PMS Channel Interface

Intercepts PMS channel interrupts, performs the requested validation, and updates the PMSSW. It passes validation control information to the MDVC.

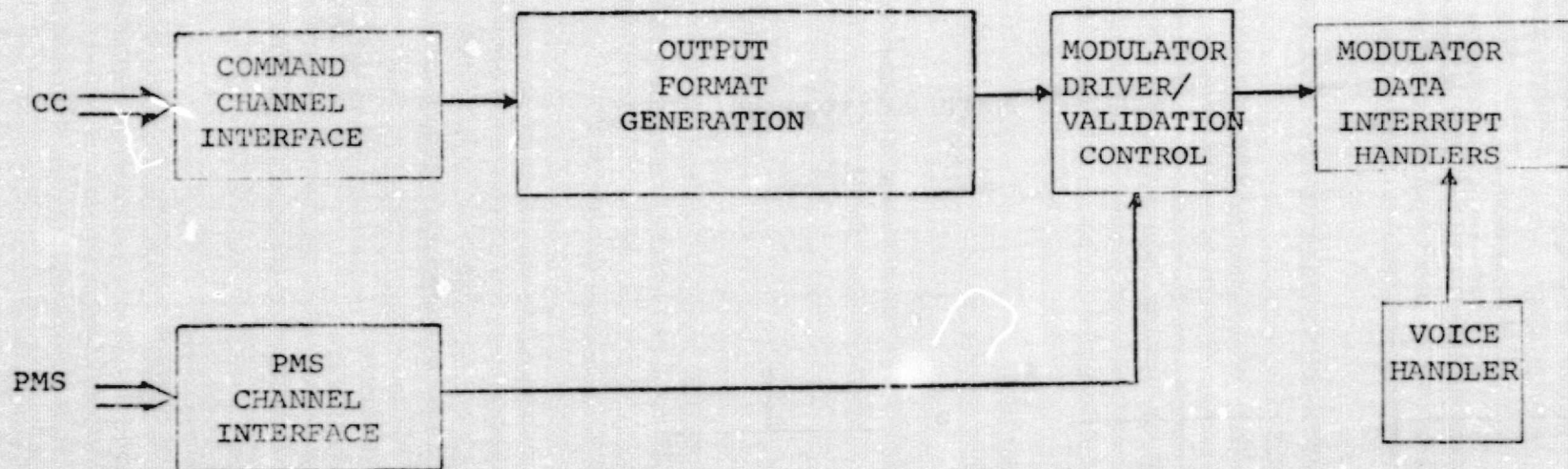


FIGURE 2 - 1

CE SOFTWARE BLOCK DIAGRAM

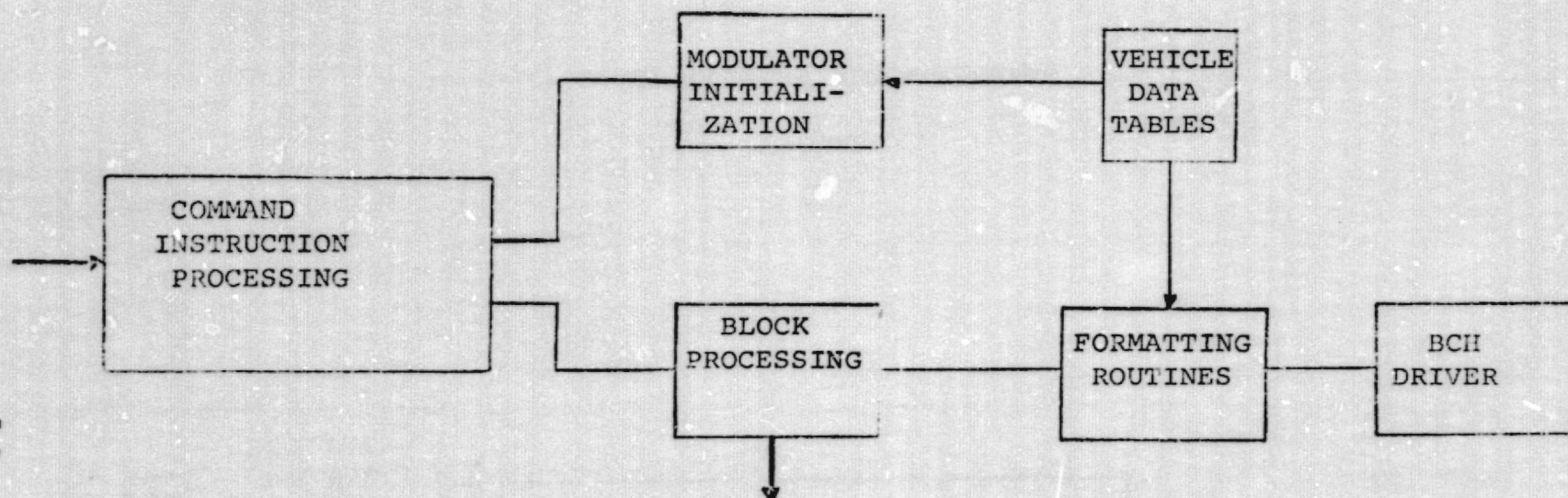


FIGURE 2-2
FORMAT GENERATION BLOCK DIAGRAM

2.5 Modulator Data Interrupt Handlers

Upon receipt of a modulator data request interrupt, it tickles the modulator appropriately: if data is available, it is transmitted; otherwise, an appropriate gap is transmitted.

2.6 Voice Interrupt Handler

Accepts voice data and places it in one of two 8-word buffers. The data is accessible by the modulator data interrupt handler for NASA 1 and 6.

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3.0 DESIGN APPROACH

The main design goal was to construct a framework which would facilitate modularization of the software tasks and allow well defined modules to be developed independently. However, execution time overhead must be minimized to prevent slowing down the modulator unit.

This goal was achieved by using simple, WAIT-SIGNAL, synchronization procedures as system primitives. In effect, these procedures channel through a single dispatcher the timing signals transferring control between tasks. This concentration of control allows the development of diagnostic routines to simulate external stimuli.* It also provides a convenient point for inserting error checks at debug time.

To minimize execution time while the Modulator is active, modulator data requests are handled asynchronously while formatting continues in background mode. In general, all interrupt handlers to data processing routine communication is buffered by the synchronizing procedures. This permits sequential processing despite the introduction of asynchronous events caused by double buffering.

3.1 Task Structure and Coroutines

Figure 3.1 details the communication between the main software modules. It also delineates the tasks and interrupt service routines which may be thought of as parallel processes or coroutines. The algorithms executed by each coroutine follows the same basic scheme:

1. Wait for an event to occur.

The event could be an interrupt such as a modulator data request, a command channel message, voice data, etc. The event could also be the indication that some other coroutine has completed an assigned function.

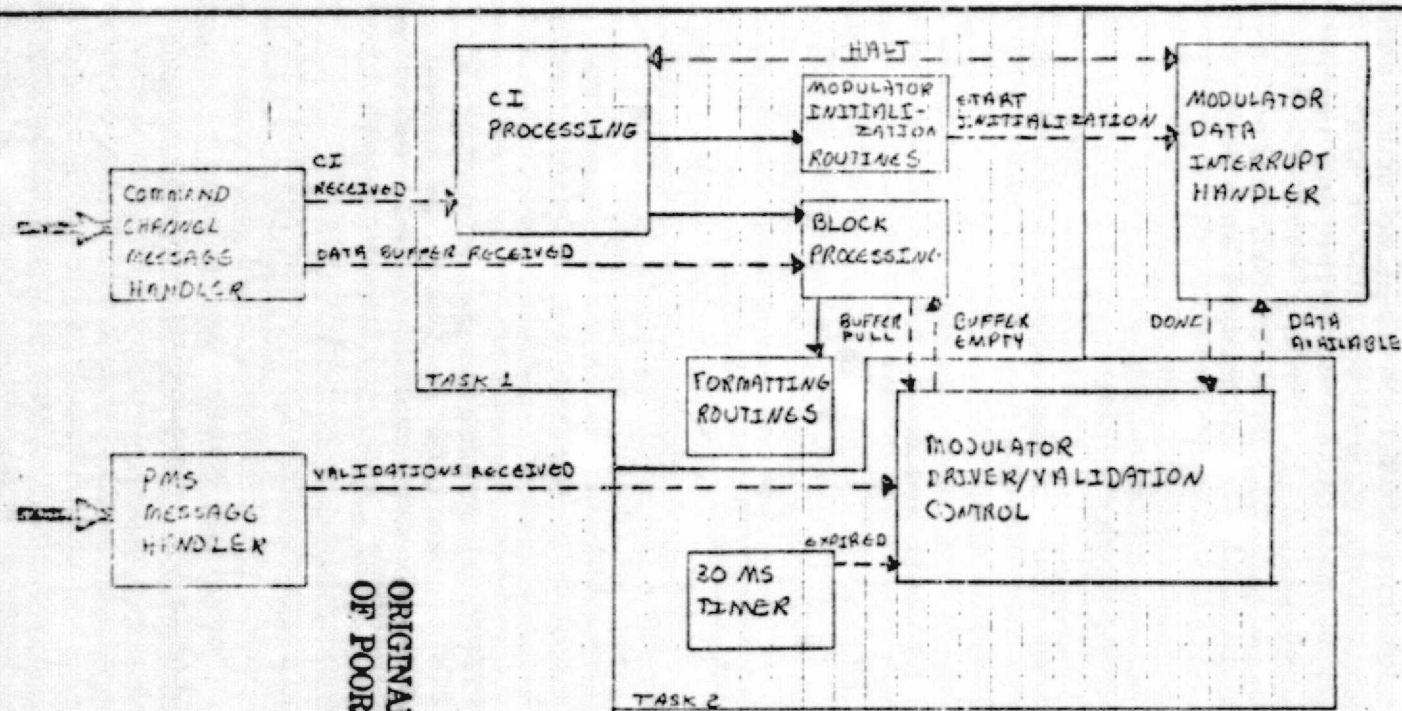
2. Perform some function.

3. Signal that the function has been done.


4. Go back to (1).

Performing a function may also require waiting for an event, leading to the more involved structures of Task 1 and Task 2.

* Not developed.



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SIGNAL 

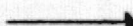
CALL 

FIGURE 3.1
COROUTINE INTERFACES

3.2 Semaphores

3.2.1 Analysis

The communication between coroutines has been simplified to the sending and receiving of timing signals to indicate that an event has occurred. Since coroutines are running essentially asynchronously more events may occur than can be acknowledged. That is, more signals may have been sent than have been received. The inverse situation is also true; the number of received signals cannot exceed the number sent. Therefore, a variable must be maintained defining the number of signals sent, but not yet received. Such a variable is called a semaphore. Also, a variable must be maintained indicating that a coroutine is waiting to receive an event.

If for some semaphore i

$S(i)$ = the number of signals sent

$R(i)$ = the number of signals received

and initially $S(i) = R(i) = 0$. Then

$$0 \leq R(i) \leq S(i) \leq R(i) + \text{max},$$

where MAX is the upper limit of integers associated with the semaphore, must always be true. Since in practice, the range of integers is much larger than the number of unconsumed signals that can occur we ignore this constraint and expound the following synchronizing rules of semaphores:

1. If the operation WAIT(i) is started at a time when $R < S(i)$, then $R(i)$ is increased by one and the receiver continues; but if $R(i) = S(i)$, then the receiver is delayed in a task queue associated with the semaphore i .
2. The operation SIGNAL(i) increases $S(i)$ by one; if one or more tasks are waiting in the queue associated with semaphore i , then one of them is selected and enabled to continue, and $R(i)$ is increased by one.

For additional detail refer to:

Brinch-Hansen, Per-Operating System Principles
Madnick, S. and Donovan J. - Operating Systems

3.2.2 Implementation

Since $R(i) \leq S(i)$ we can replace these two variables by a single variable P where

and $P(i) = 0$ when $R(i) = S(i)$
 $P(i) > 0$ when $R(i) < S(i)$

If $P(i)$ is negative, $|P(i)|$ represents the number of tasks waiting for an event. (In the present Command Encoder System, this will never be greater than one.) Therefore, the Wait and Signal functions are redefined as follows:

1. The WAIT(i) operation decreases $P(i)$ by one; if $P(i) < 0$ the receiver continues; if $P(i) \geq 0$ the receiver is placed on the task queue associated with semaphore 1.
2. The SIGNAL(i) operation increases $P(i)$ by one, if $P(i) \leq 0$ a task is taken off the semaphore (i) queue and enabled to continue.

Since semaphores are common variables, operations which modify them must be excluded in time. Therefore, both the WAIT and SIGNAL functions run with interrupts disabled.

3.3 Coroutine Outlines

The following descriptions are rough outlines of the coroutine logic. They are intended only to demonstrate the communication between the coroutines. Figure 3.2 shows a detailed operational flow with processing overlap indicated.

3.3.1 Command Channel Message Handler

1. Wait for CCMSG interrupt.*
2. Check for valid CCMSG word. If invalid set proper status bit and GO to (4).
3. Signal (XSNCI) to indicate that a Command Instruction has been received, and/or Signal (XSNDB) to indicate that a new Data Block has been received.
4. GO BACK TO (1).

3.3.2 TASK 1

1. Wait (XSNCI) for a new CI to be sent.

* This corresponds to enabling the correct level interrupt.

COMMAND CHANNEL	COMMAND INITIALIZATION CHECK CCSW SEND CI SEND DB SEND CCMG			CHECK STATUS	SEND NEXT DATA BLOCK SEND CCMG						
COMMAND CHANNEL MESSAGE INTERRUPT HANDLER (INTERRUPT DRIVEN)		DECODE CCMG SIGNAL CODING AND FORMAT GENERATOR			DECODE CCMG SIGNAL CODING AND FORMAT GENERATOR						
CODING AND FORMAT GENERATION MODULE (SWAPHORE DRIVEN)			DECODE CI SWAP CI BUFFERS UPDATE CCSW INITIALIZE MODULATOR	SWAP DB BUFFERS UPDATE CCSW FORMAT AND ENCODE 2 COMMAND WORD				FORMAT AND ENCODE 1 COMMAND WORD			
MODULATOR INTERRUPT HANDLER (INTERRUPT DRIVEN)				OUTPUT INITIALIZATION SEQUENCE	OUTPUT COMMAND WORD TO MODULATOR	OUTPUT NULLS, SPACE, BLANK, etc.	OUTPUT NULLS, SPACE, BLANK, etc.	OUTPUT NEXT COMMAND WORD			
PMS MESSAGE INTERRUPT HANDLER (INTERRUPT DRIVEN)							DECODE PMS MSG PERFORM VALIDATION UPDATE PMSW				
PERFORMANCE MONITOR SYSTEM					RECEIVE VALIDATION DATA	CHECK PMS STATUS WORD SEND DATA SEND PMS PSC		RECEIVE VALIDATION DATA			

FIGURE 3.2 DETAILED OPERATIONAL PROCESSING FLOW

REPEAT UNTIL ALL BLOCKS PROCESSED

REPEAT UNTIL BLOCK COMPLETED

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2. Check for a valid CI; if invalid set proper status bit and go to (4). Decode CI and initialize modulator.
3. (a) WAIT (XSNDB) for a new Data Block to be sent.
(b) Check for valid word count; if invalid set proper status bit and go to (a).
(c) (i) WAIT (XSMTY) for an empty output record buffer.
(ii) Format an input record.
(iii) SIGNAL (XSFUL) that a buffer is full.
(iiii) If that was the last record in the block go to (d); else go to (i).
(d) If that was the last block, go to (4); else go to (a).
4. Go to (1).

3.3.3 TASK 2

1. Wait (XSFUL) for a full output buffer.
2. (a) Send data to Modulator Data Interrupt Handler (MDIH).
(b) Wait (XSMDTA) for a data request from MDIH.
(c) If validations necessary, set up PMSSW and start timer.
(d) Wait (XSTIMR) for timer runout or validation complete signal.
(e) If validations fail and re-send 0 go to (a).
3. Signal (XSMTY) to indicate that buffer is available for more data.
4. Go to (1).

3.3.4 PMS Message Handler

1. Wait for a PMSMSG interrupt.
2. (a) Check for a valid PMSMSG, if invalid set proper status bit and go to (1).
(b) Perform requested validations and set status bits accordingly.
3. If all validations have been performed, signal (XSTIMR).
4. Go to (1).

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3.3.5 Modulator Data Interrupt Handler

1. Wait for modulator data interrupt.
2. If data available, send next unit of data to modulator, and go to (3). Else send appropriate null data and go to (1).
3. If that was the last unit in buffer, SIGNAL (XSMDTA) to request more data.
4. Go to (1).

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4.0 Detailed Flowchart Description

4.1.1 Initialization and Dispatcher

At system initialization, the I/O buffer memory area (Figure 1.3) and the TCB and semaphore area (Figure 4.1) are set to the initial state. The dispatcher (XDISP, Figure 4.2) is then entered. This routine gets the address of the first TCB and checks if it is blocked. Since it is not, the address of the TCB is placed in XDDRUN, indicating that it is running (active). The contents of the register save area of the TCB (Figure 4.4) are placed in the appropriate registers and execution is transferred to the new command instruction (NCI) processing routine.

4.1.2 Semaphore Wait Operation

The NCI (Figure 4.5) routines first action is to check if there exists a command instruction. This is accomplished by performing a WAIT operation on the new command instruction semaphore (XSNCI). The XWAIT routine (Figure 4.3) decrements the count field of the given semaphore and checks its contents. If the value is negative, nothing is available and so the calling routine is blocked from further processing. This is done by setting the blocked bit in the TCB whose address is in XDDRUN. The register contents at entry to XWAIT are saved in the TCB in the appropriate slots, the address of the TCB is placed in the first SEMAPHORE WAITER field of the given semaphore, and control is returned to the dispatcher.

XDISP next finds that the second TCB is not blocked and starts it (MDVC). MDVC (Figure 4.7) performs a WAIT on the buffer full semaphore, XSFUL, and a sequence identical to the above is performed. However, at this time, XDISP finds no TCB that is unblocked and so repeats the sequence.

4.1.3 Command Channel Interrupt Service

Eventually, a CI and a data block (DB) will be transmitted to the CE and followed by a Command Channel Message (see Figure 4.9 for handshaking conventions). The CCMSG causes an interrupt to the CE processor which transfers control to the Command Channel Interrupt Service (CCIS) routine (Figure 4.8). The first check made by this routine is to determine whether the CCMSG is a HIGH PRIORITY indication, which would abort any ongoing processing. If not a HIPRI, the CI request bit is checked in the CCSW. If the request bit is set and we do not get a CI, something is wrong. If the CI was sent, a

SIGNAL operation is performed on XSNCI and the CI request bit is reset. Since the DB request bit is always set whenever the CI request bit is set, we check if a DB was transmitted. If so, a SIGNAL is performed on XSNDB and the request bit is reset. On exiting control is returned to the previously running routine.

4.1.4 Semaphore Signal Operation

The SIGNAL routine (XXSIG, Figure 4.3) increments the count field of the given semaphore. If the resultant is zero, or negative, it indicates that someone is waiting for this signal. In that case, the first TCB WAITER (which is a TCB address) has its blocked bit reset and is removed from the wait list.

4.1.5 Command Instruction Processing (A)

The dispatcher (XDISP) finds the TCB unlocked and resumes the task with the appropriate register contents as stored in the TCB. This restarts the NCI (Figure 4.5a) immediately following the WAIT operation. Then, miscellaneous initializations are performed and CI validity checks made. If the CI is valid, it is disassembled and placed in the working CI buffer. The CE 'busy' bit is set and the appropriate modulator initialization routine is called.

4.1.6 NASA 1 Modulator Initialization

Figure 4.10 shows the NASA 1 Modulator initialization routine (INASAl). This routine sets, appropriately, flags and an interrupt count for the one second of ones. The modulator control register and synthesizer registers are also set accordingly. The path control flag (PCF) is set for repeat, the next path control flag (NXTPCF) is set for the INIT path. The modulator data buffer is set to all ones. The modulator "M" counter is set to 0 and the "N" counter is set to 16. Just before returning to NCI, the modulator's START bit is set; thereby starting the modulator processing on the data buffer, which immediately causes the first data request interrupt.

The modulator interrupt causes control to be transferred to the modulator data interrupt handler (Figure 4.11) which uses the PCF to determine which path to follow. Since the PCF was set for REPEAT in INASAl, the modulator word count (MWC) is decremented and, if not zero, a normal interrupt return is made (i.e., enable interrupts and return to previously running routine with proper register contents).

4.1.7 Command Instruction Processing (B)

NCI is eventually returned control and, after some miscellaneous initializations, checks to see if a DB is available. This is done by performing a WAIT operation on XSNDDB (Figure 4.5b). Since a SIGNAL operation had previously been performed by CCIS, the WAIT operation returns immediately. If the word count is valid, the DB buffer addresses are swapped with the second DB buffer and the DB request bit is set. The temporary block count (TBC) is incremented and the block processing routine (BLKCTL) is called.

4.1.8 Block Processing and Formatting

BLKCTL (Figure 4.6) controls the processing of the command words within a block. After miscellaneous initializations, a WAIT is performed on XSMTY (wait for buffer empty). This wait returns immediately. (This semaphore was initialized to 2 (Figure 4.1) indicating that 2 empty buffers are available). Therefore, the next empty buffer is taken for use. The address of this buffer (the "output buffer") is passed to the proper formatting routine along with the address of the current input data word.

The NASA 1 formatting routine (FNASAL, Figure 4.12) takes the vehicle address and the system address from the CI working buffer and left justifies them in the output buffer. Next, 40 bits of data are transferred from the input data buffer to the output buffer. The address of the buffer is then sent to the BCH encoder driver which does the encoding and returns with the parity bits in the output buffer. The formatting routine then returns to BLKCTL.

BLKCTL then performs a signal on the buffer full semaphore (XSFUL) which discovers a waiting task and unblocks it. If the data in the DB is not exhausted, the input buffer pointer is advanced to the next input data word. The WAIT-FOR-EMPTY to SIGNAL-THAT-FULL cycle is repeated until all available buffers are filled (in the current system, this count is 2). The next WAIT then causes BLKCTL to be blocked until a buffer is emptied by the modulator driver. Eventually, the DB is exhausted. Enough WAITS are performed on XSMTY to ensure that the last filled buffer has been transmitted. Then the verified block count (VBC) field on the CCSW is updated, if appropriate.

BLKCTL then returns to NCI which will loop through the entire cycle until all specified data blocks have been processed. Just before starting processing the last block, the CI request bit is set, in the CCSW, allowing a new CI to be sent while

the last one is still being processed. When the last block is complete, if it was a NASA 1, 2, or DOD type CI, the Halt flat is set and we wait for a new CI. Otherwise, the modulator is halted and we wait for a new CI.

4.1.9 Modulator Driver/Validation Control

When BLKCTL was waiting for an empty buffer, the dispatcher gave control to the modulator driver/validation control task (MDVC Figure 4.7). Control was returned to the point immediately following the WAIT-On-BUFFER-FULL operation, indicating that a buffer is, indeed, full. The address of the buffer is retrieved, temporary transmit count (TTC) is initialized, and the modulator interrupt handler data buffer pointer is set to the full buffer. Then MDVC waits for the modulator interrupt handler to indicate that the buffer data has been transmitted. If validations had been requested, the TTC is decremented, the 30 ms timer is started, and the task waits for XSTIMR.

Control is returned when (1) all requested validations have been completed, or (2) when the 30 ms. timer runs out. If validation has failed or if the timer runs out, the buffer is retransmitted until TTC goes to zero. When the buffer has been transmitted for the last time, a signal is performed on XSMTY and the cycle starts over.

4.1.10 Modulator Data Interrupt Handler For NASA 1 (MDIHN1)

During the time that BLKCTL was formatting and filling the first two buffers, MDIHN1 (Figure 4.11) was being given control approximately every 400 sec. (Assuming NASA 1 with voice.) For 2492 interrupts it simply decremented, the MWC and returned to the currently running routine (repeat path). On the next interrupt, it enabled the digital voice interface (INIT PATH). On the 2500th interrupt, the path control flag (PCF) is set for the SYNC path and the MWC is set to 2. The first time through the SYNC path, the MWC is decremented and, since it is not zero, the first half of the sync code is loaded into the modulator data buffer. The second time through, MWC is decremented to zero. Since the voice flag is set, the PCF is set to VOICE, NXTPCF is set to DATA, MWC is set to 8 and the modulator data buffer is loaded with the second half of the sync code.

The VOICE path is then taken for 8 times. On the eight entry, the PCF is set to the contents of the NXTPCF and the MWC is set to 2. This will cause control, in this case, to transfer to the DATA path. The DATA path will output two words (16-bit) from the output buffer and return control to the VOICE path

placing DATA as the NXTPCF until $DWC = 0$. Then the NXTPCF is set to SYNC, the PMS initialization routine is called to allow validation data transfers, a signal is performed on XSMDTA to indicate to MDVC that the output buffer has been transmitted, the data available flag is reset (BUFPTR), the NULL flag is reset, and the DWC is set to 8 (to ensure that 128 zeros are sent in the event that data is unavailable when the data path is again taken.)

The MDIHN1 continues until the halt flag is set. An orderly shutdown is then executed ending with a signal on XSMHLT indicating that the modulator is, indeed, turned off.

4.1.11 PMS Channel Routines

When the modulator data interrupt handler had completed transmitting on output word, it called the PMS initialization routine. This routine checks the CI working buffer to determine if validations had been requested, and if so, sets appropriate flags for MDVC and the PMS Interrupt Service (PCIS) routine (Figure 4.13).

When the AUX computer receives validation feedback, it determines which validations have been requested and transmits the proper data using the PMS Channel Handshaking Conventions (Figure 4.14). When PCIS receives the PMS MSG and associated data, it checks if the given validation data was requested. If so, the comparison of the appropriate input buffer with the current output buffer is made. The PMS Status Word (PMSSW) is updated appropriately, as well as flags for MDVC.

When all validations have been received, the 30 ms timer is stopped. A SIGNAL operation is performed on XSTIMR to inform MDVC of the validation completion.

4.2 TRANSPARENT MODE DESCRIPTION

A transparent data mode is provided for all transmission types except NASA 3 and NASA 4.

4.2.1 NASA 1, NASA 6

If the transparent mode bit is set in a NASA 1 or NASA 6 CI, the word count is interpreted as the number of contiguous 160-bit words in the DB. (NOTE: The word count field of the CI starts at zero. Zero indicates one word.)

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4.2.2 NASA 2, DOD

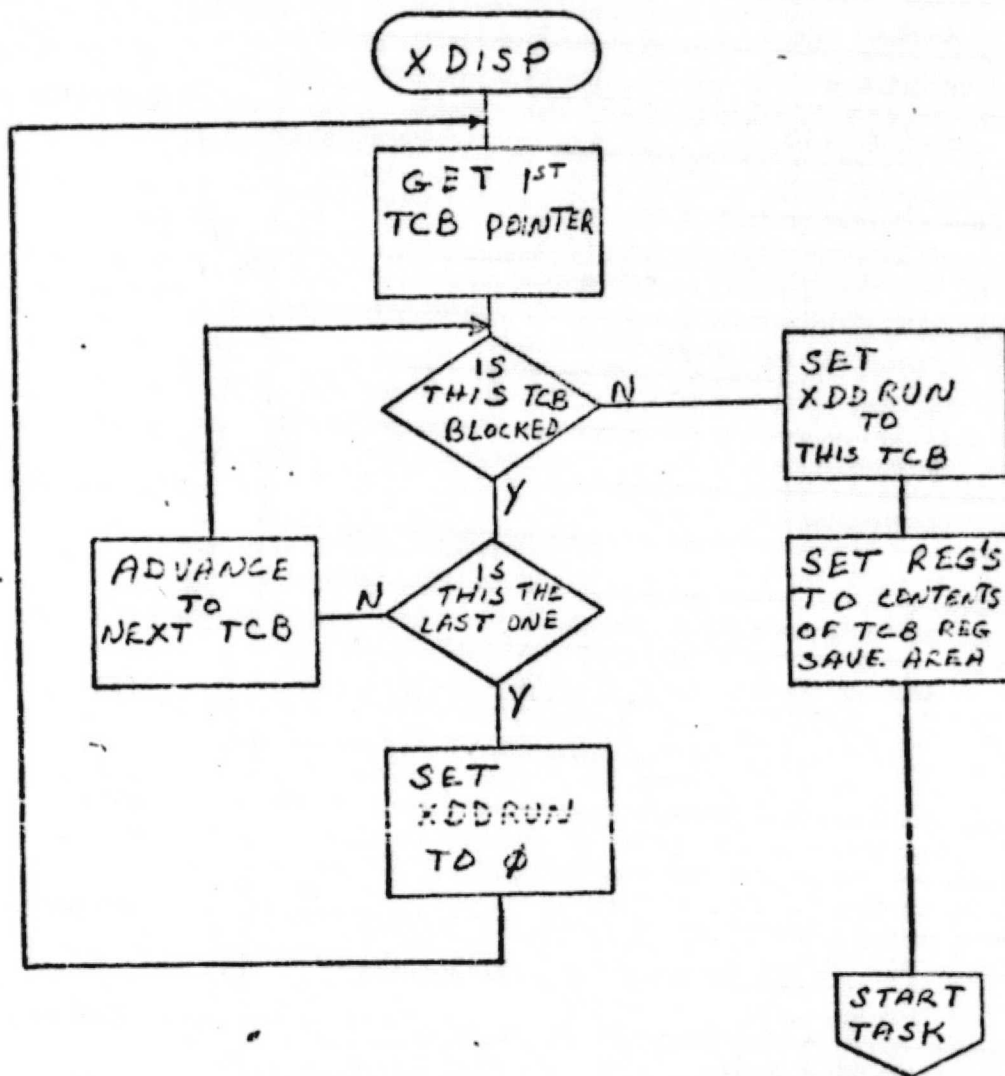
In transparent mode, the TYPE code for DOD's is meaningless. Any DOD TYPE in transparent mode will cause the special parameters field to be interpreted as the word length. The word count is interpreted as the number of the specified length words in the buffer. The word length must be a multiple of 16 bits. The above is also true for NASA 2.

4.2.3 NASA 5 transparent mode is invoked using format type 12₁₀. Note that the special parameters field specifies the output word length plus 7 for this type.

0	0		1st TCB
ADDRESS OF NCI			
A-REG = 0			
E-REG = 0			
B-REG = 0			
X-REG = 0			
WAITER = 0			
1	0		LAST TCB
ADDRESS OF MDVC			
A-REG = 0			
E-REG = 0			
B-REG = 0			
X-REG = 0			
WAITER = 0			
COUNT = 0			XSNCI
WAITER = 0			
COUNT = 0			XSNDB
WAITER = 0			
COUNT = 2			XSMTY
WAITER = 0			
COUNT = 0			XSFUL
WAITER = 0			
COUNT = 0			XSMHLT
WAITER = 0			
COUNT = 0			XSMDTA
WAITER = 0			

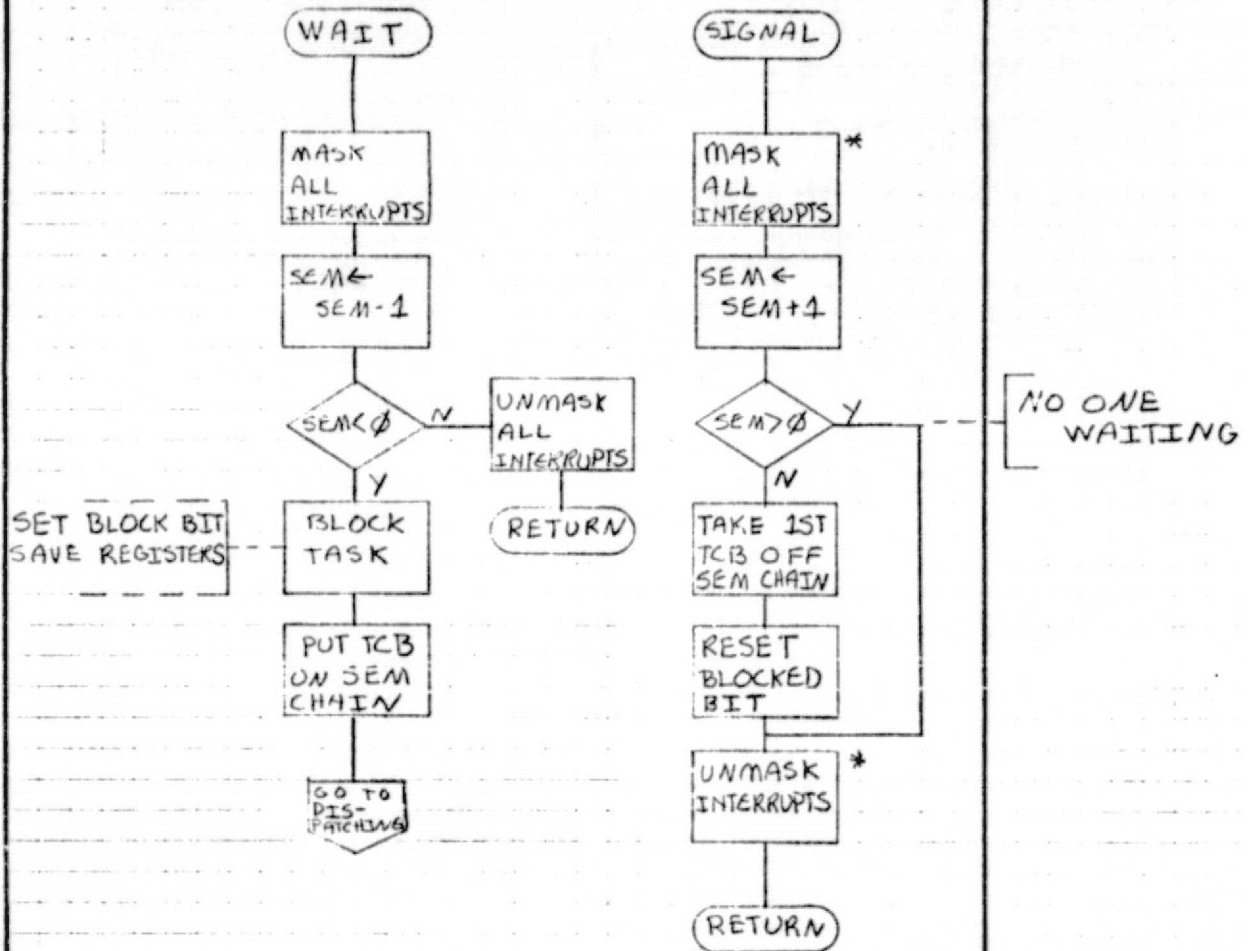
INITIAL STATE OF TCP'S AND SEMAPHORES

FIGURE 4.1



DISPATCHER

Figure 4.2



ENTRY

(ACR) = ADDRESS OF SEMAPHORE

CALL XWAIT OR XSIG
OR XXSIG

* OMIT IN
XXSIG

FIG. 4.3

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RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02173	
PROGRAM ROUTINE: WAIT/SIGNAL ROUTINES			
49956	APPROVED BY J.B. JONES	DATE 20 MAR 75	

TASK CONTROL BLOCK

15	14	7	0
EOT	Block		OVERFLOW STATUS
P-REGISTER			
A-REGISTER			
E-REGISTER			
X-REGISTER			
B-REGISTER			
NEXT SEMAPHORE WAITER			

XDDRUN

RUNNING TCB

SEMAPHORE BLOCK

COUNT
FIRST SEMAPHORE WAITER

Figure 4.4

16 APR 75

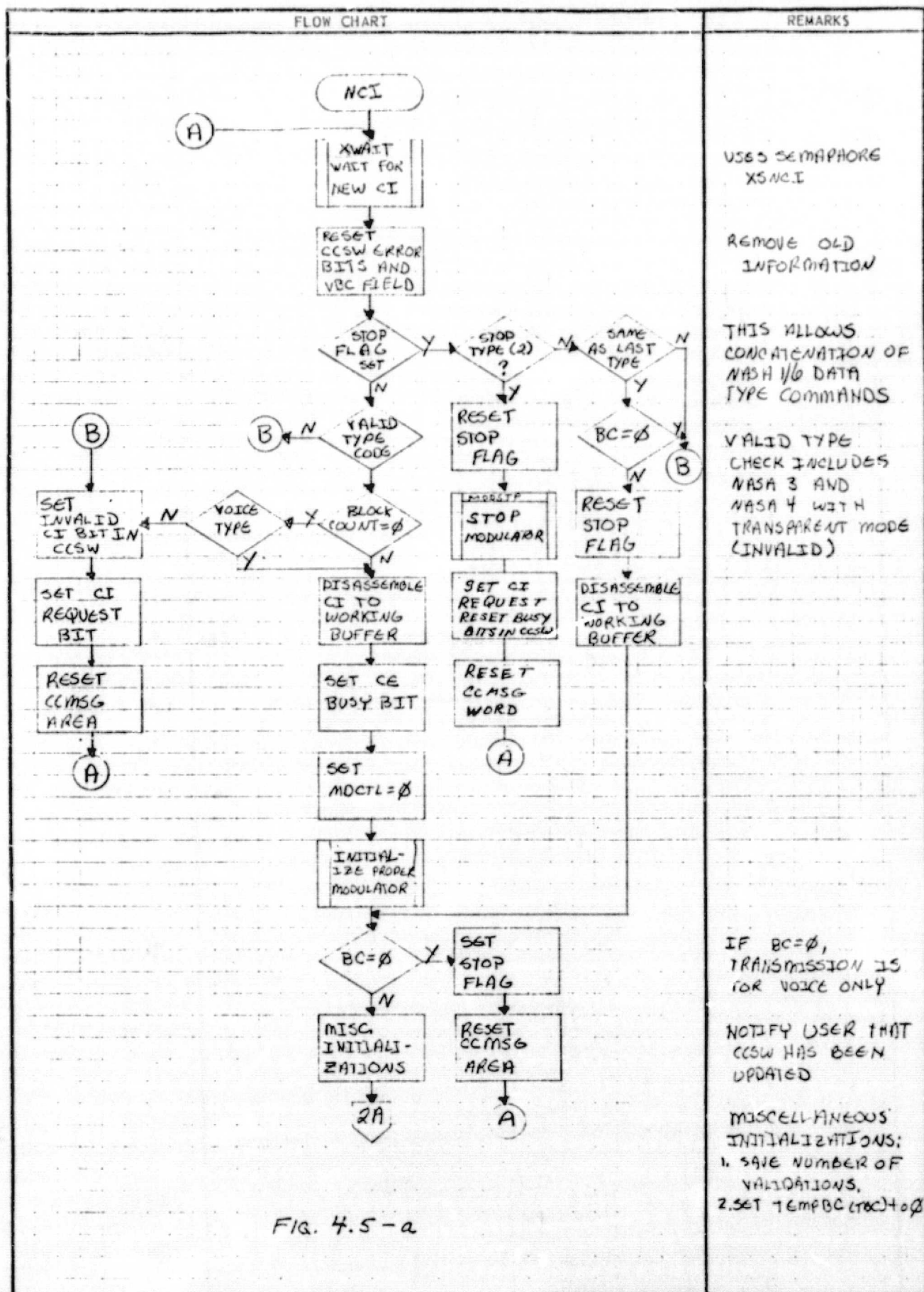
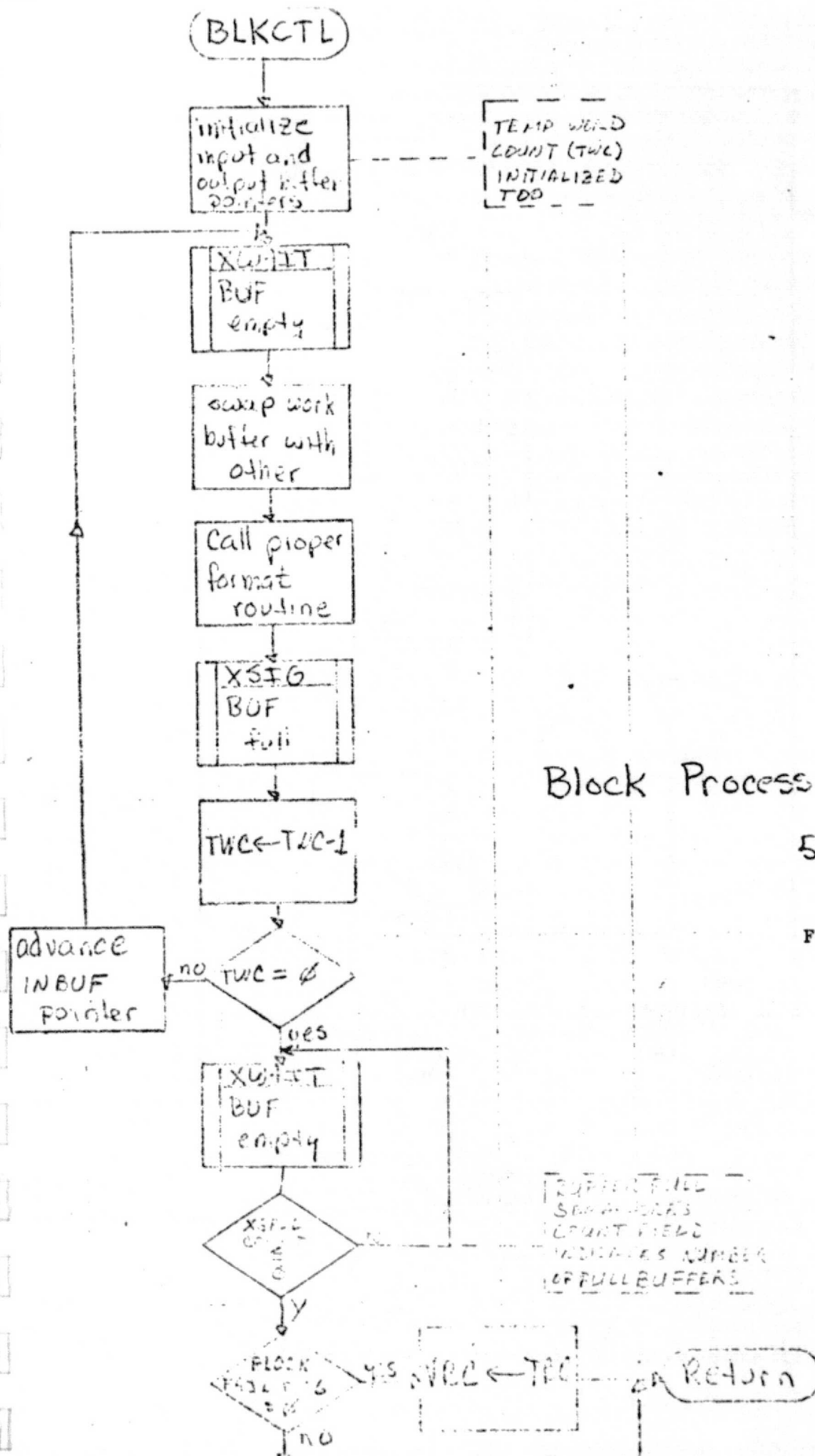


FIG. 4.5-a

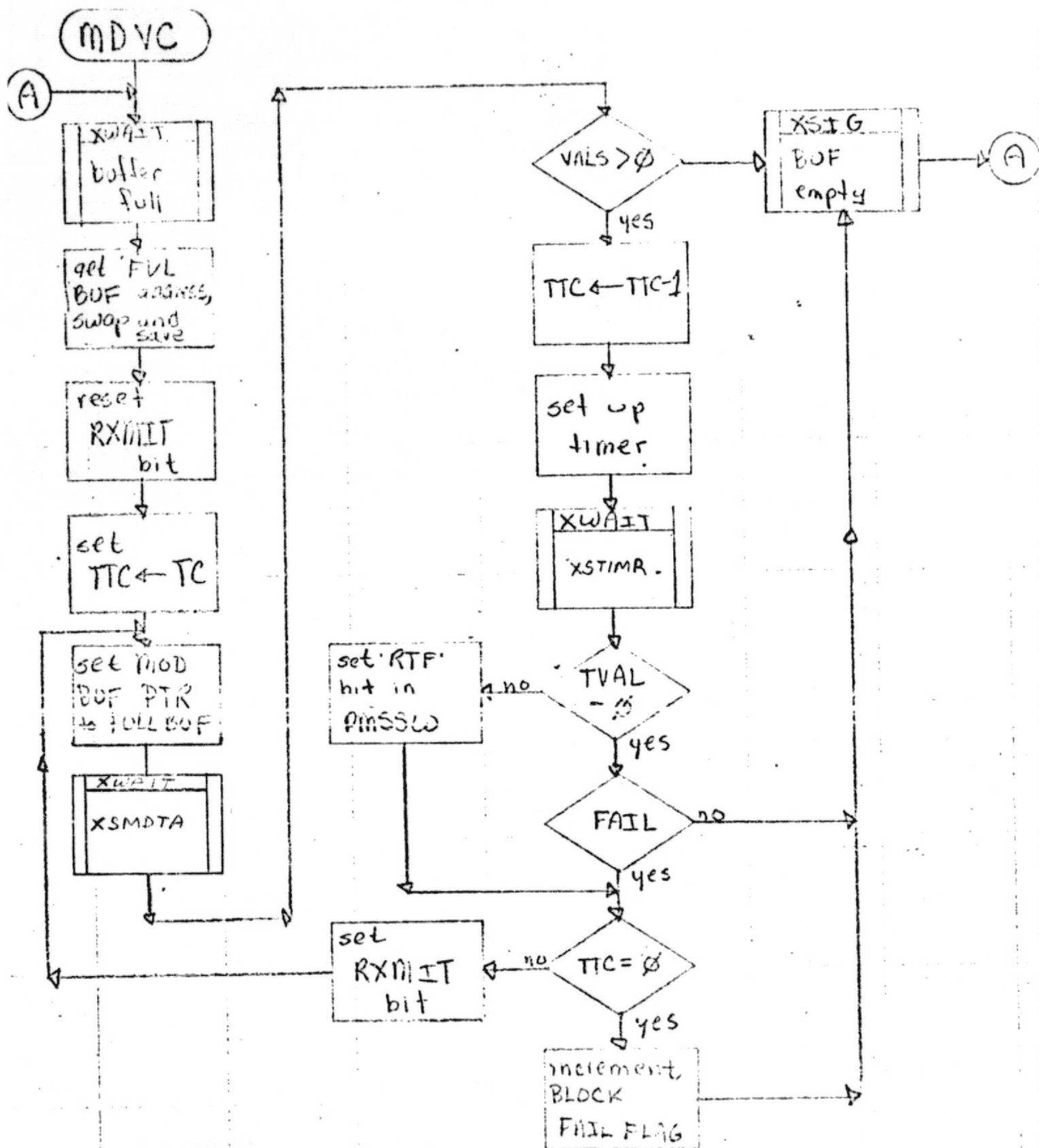
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Block Processing Control

5 April 75

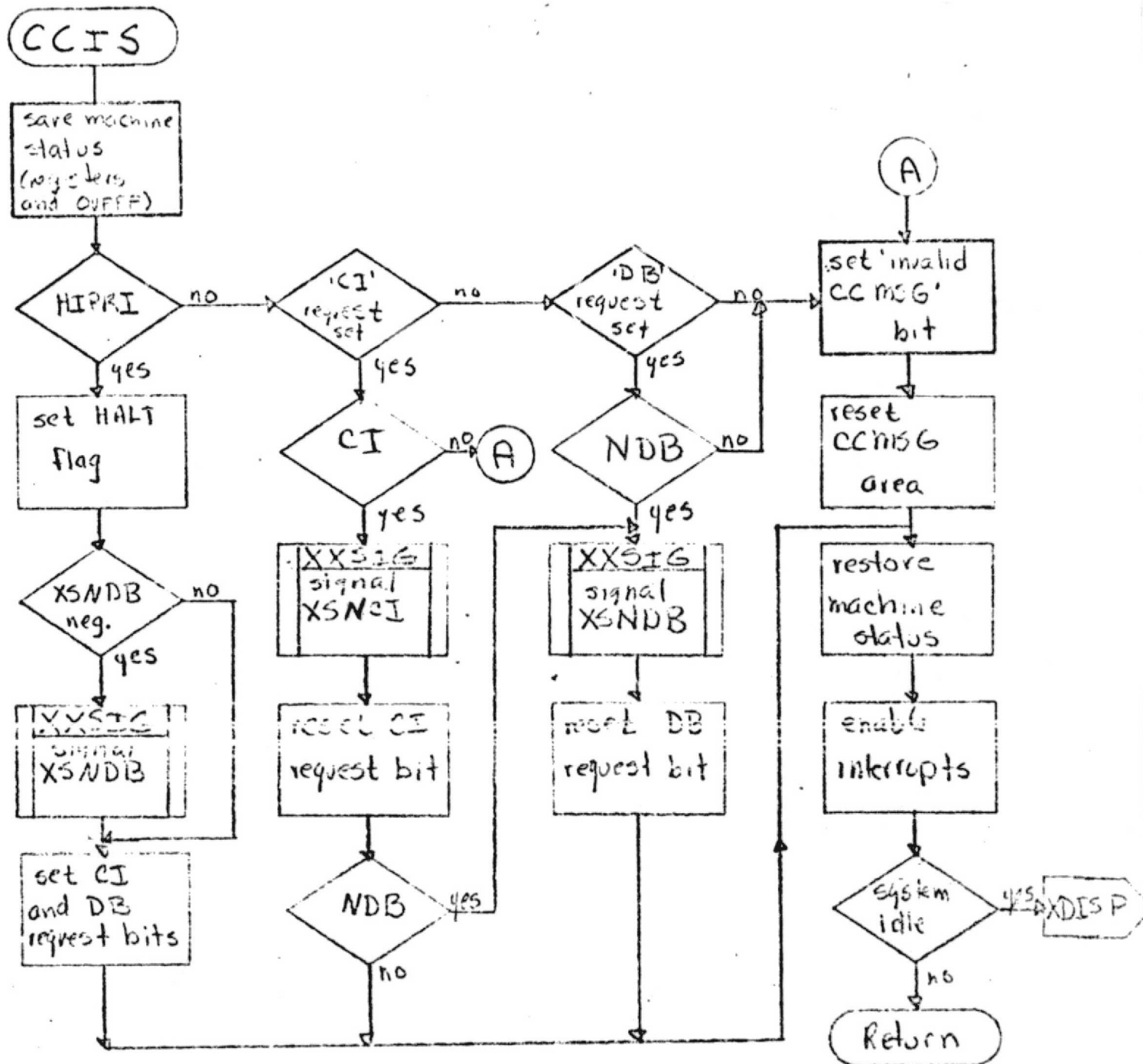
Figure 4.6



Modulator Driver and Validation Control

Figure 4.7

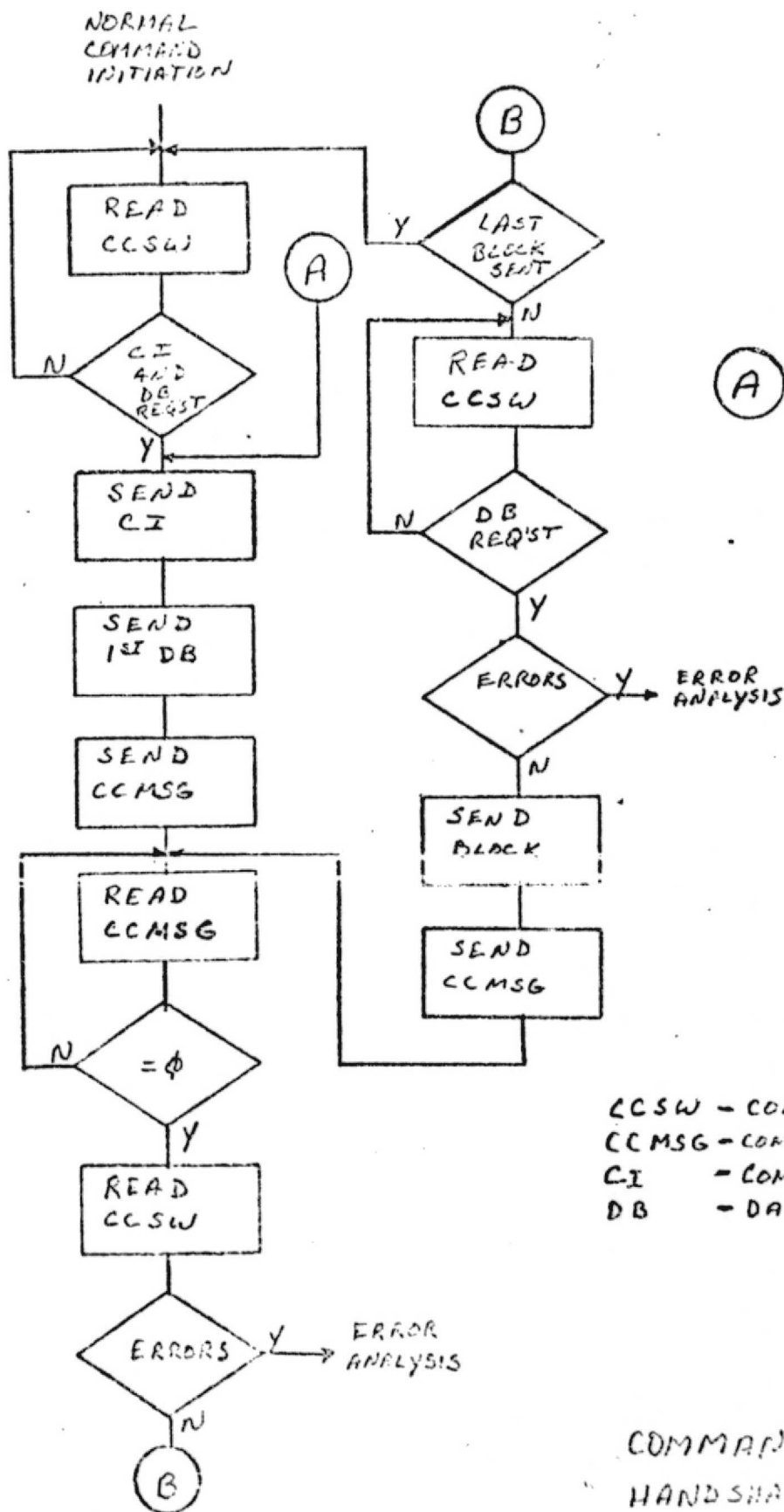
5 April 70



Command Channel Interrupt Service

Figure 4.8

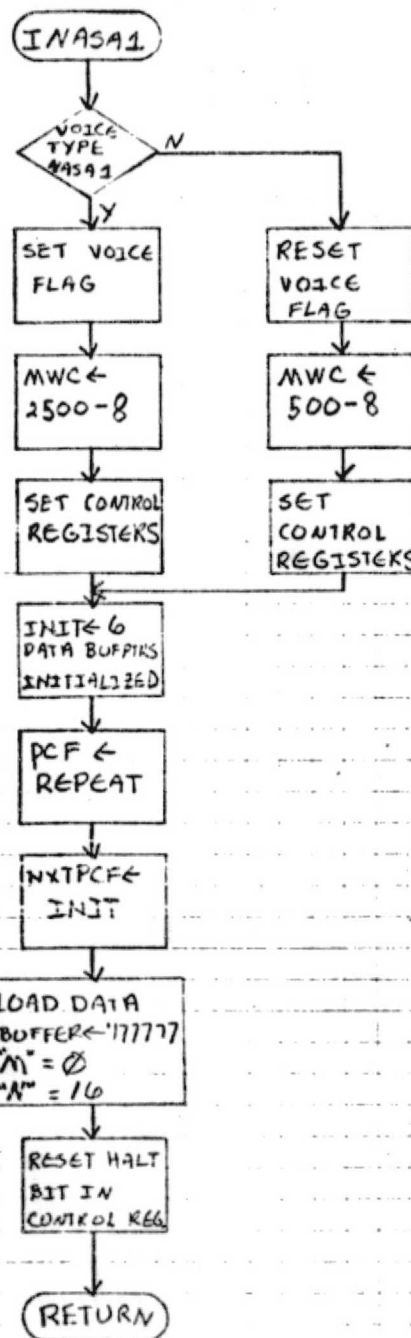
ORIGINAL PAGE IS
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CCSW - COMMAND CHANNEL STATUS WORD
 CCMSG - COMMAND CHANNEL MESSAGE WORD
 CI - COMMAND INSTRUCTION
 DB - DATA BLOCK

COMMAND CHANNEL
 HANDSHAKING 22 APR 75

Figure 4.9



MWC- MODULATOR
WORD
COUNT

2500 = 1 SEC.
AT 40 KHZ

500 = 1 SEC.
AT 8 KHZ

PCF- PATH
CONTROL
FLAG

NXTPCF- NEXT
PATH
CONTROL
FLAG

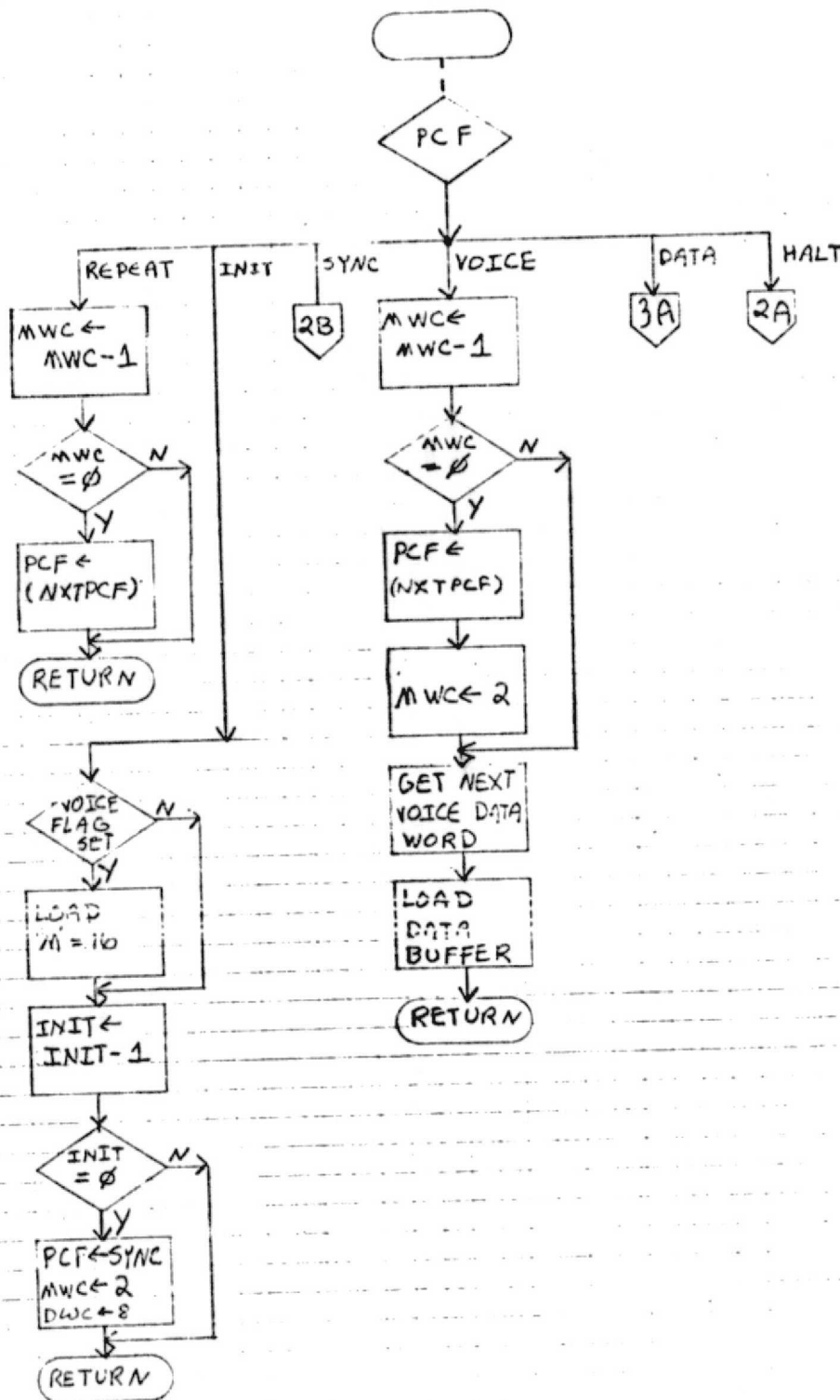
"M"-MODULATOR
M COUNT
REGISTER

"N"- MODULATOR
N COUNT
REGISTER

Figure 4.10

ORIGINAL PAGE IS
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RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02173	
VASA 1 INITIALIZATION			
49956	10 JUN 65	24 JUN 75	
REVISED		SHEET 1 OF 1	



PCF - PATH
CONTROL
FLAG

MWC - MODULATOR
WORD
COUNT

NXTPCF - NEXT
PATH
CONTROL
FLAG

"M" - MODULATOR
M COUNT
REGISTER

Figure 4.11a

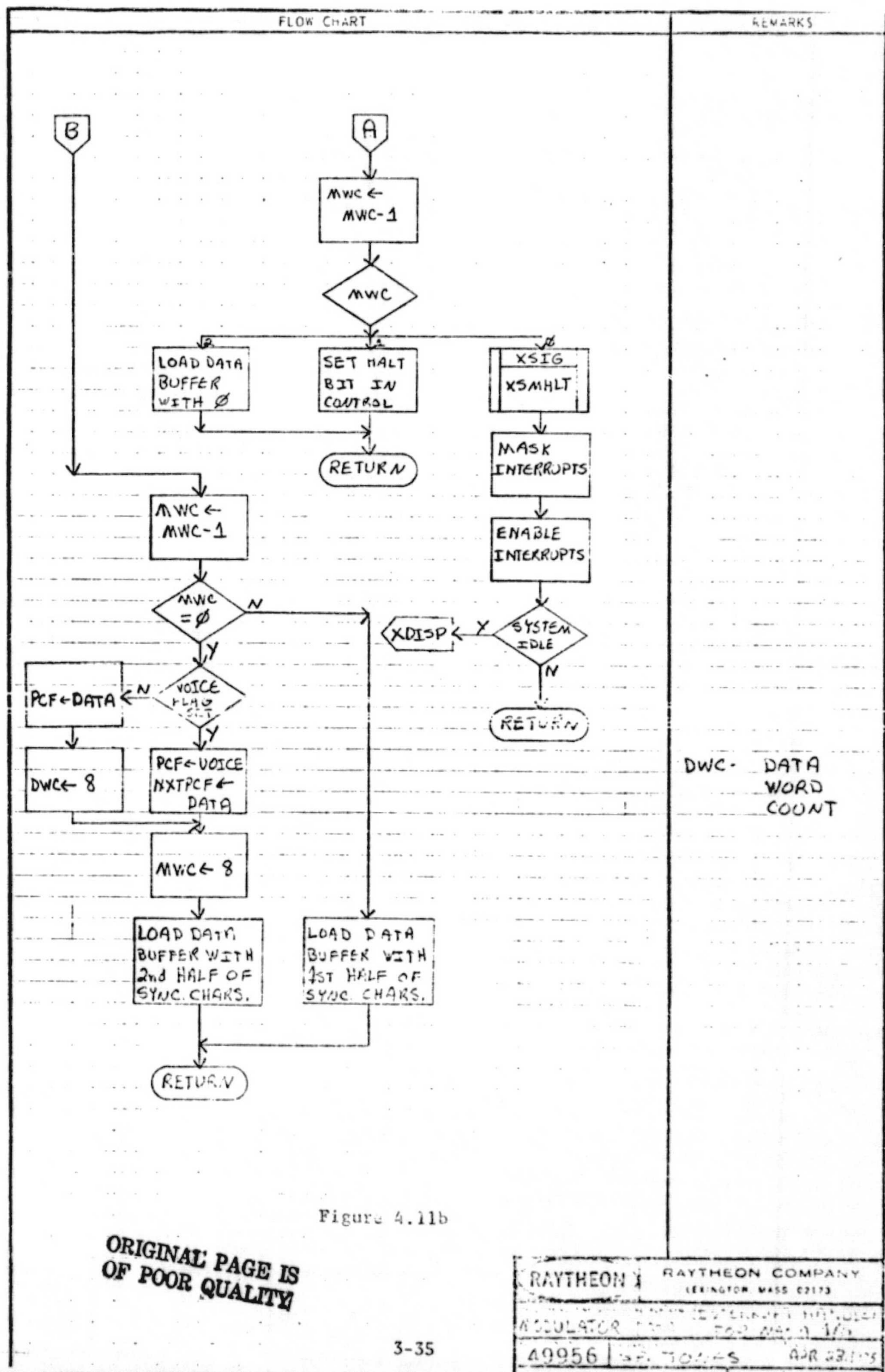
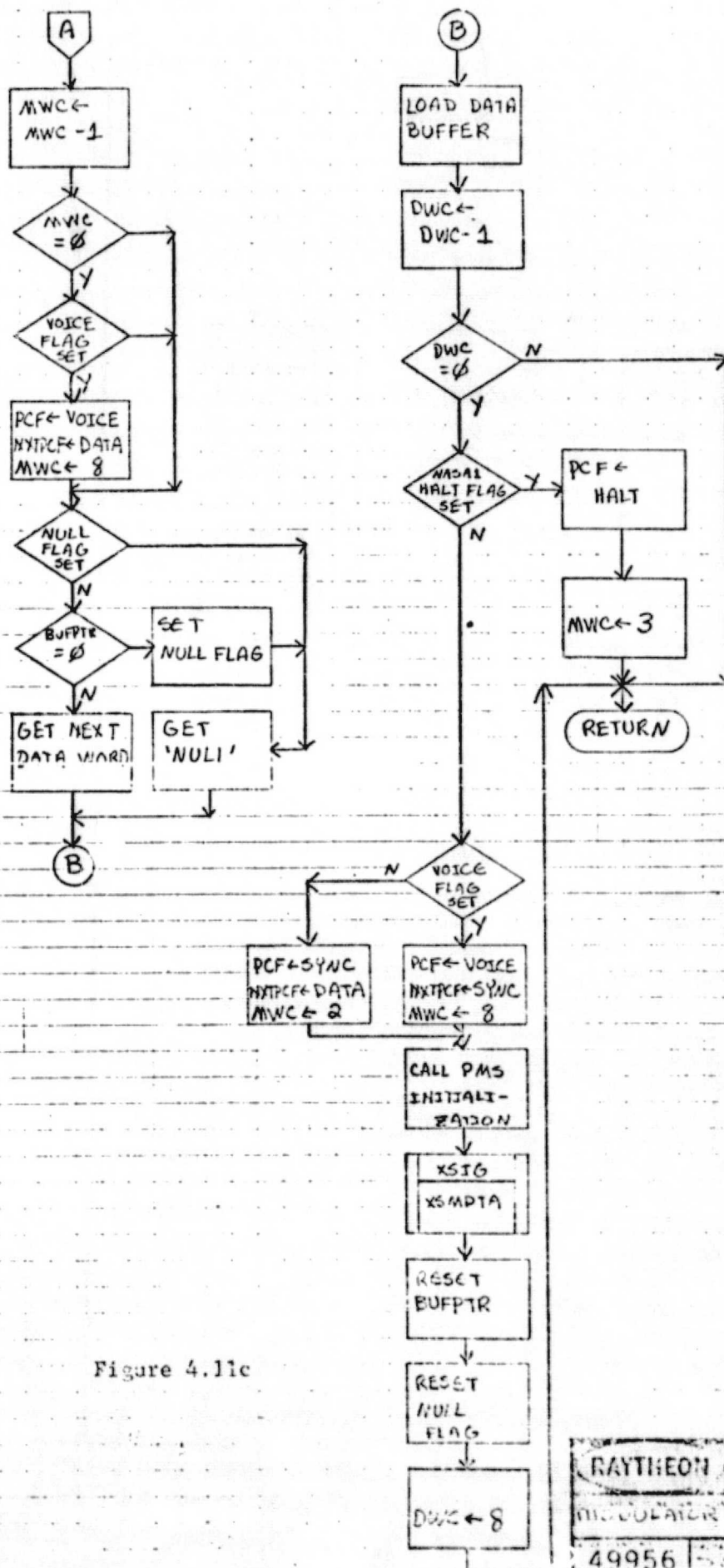


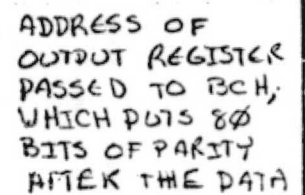
Figure 4.11b

ORIGINAL PAGE IS
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BUFPTR = 0
SIGNIFIES
NO DATA IN
BUFFER

Figure 4.11c



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PMS CHANNEL INTERRUPT SERVICE

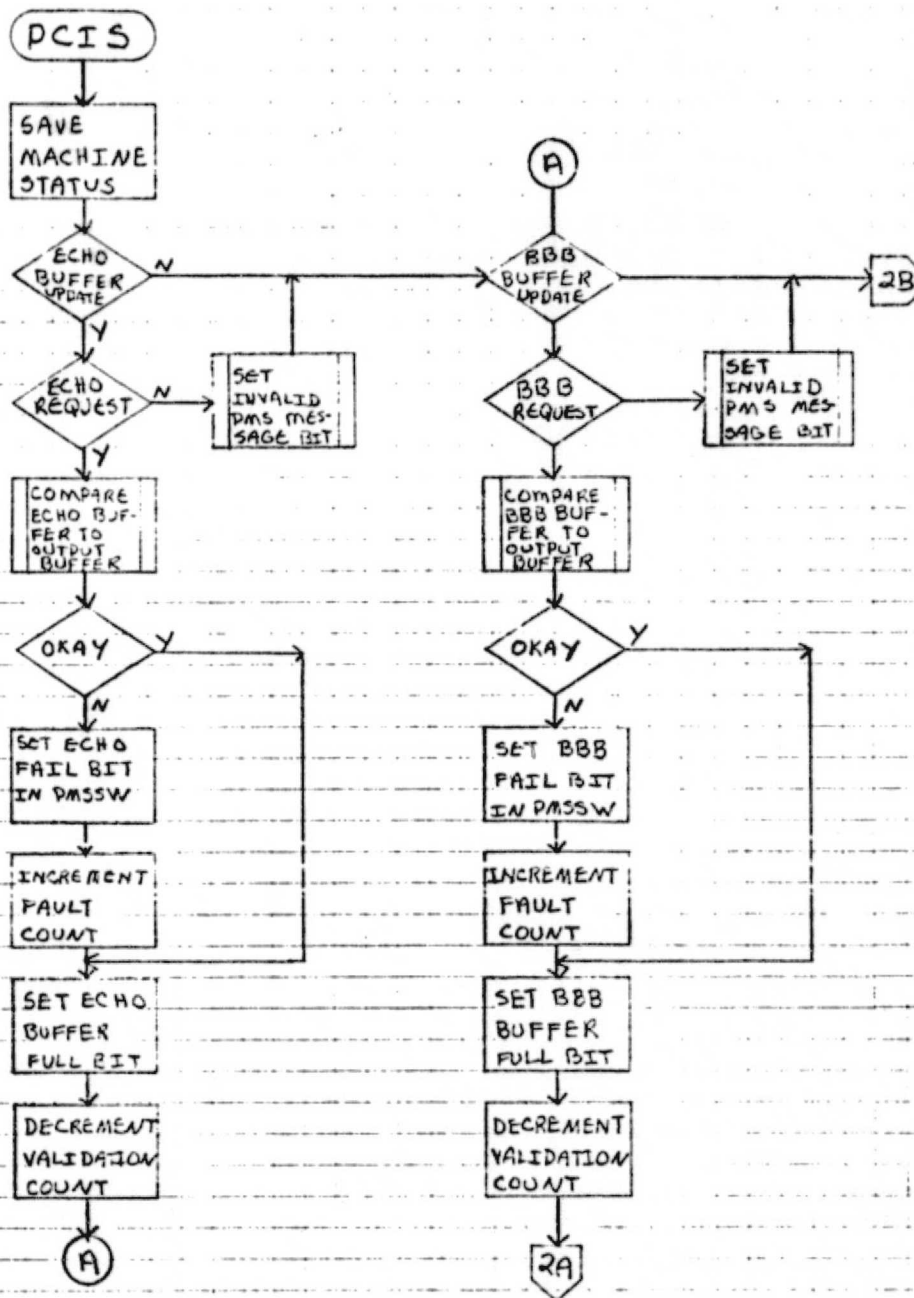


Figure 4.13a

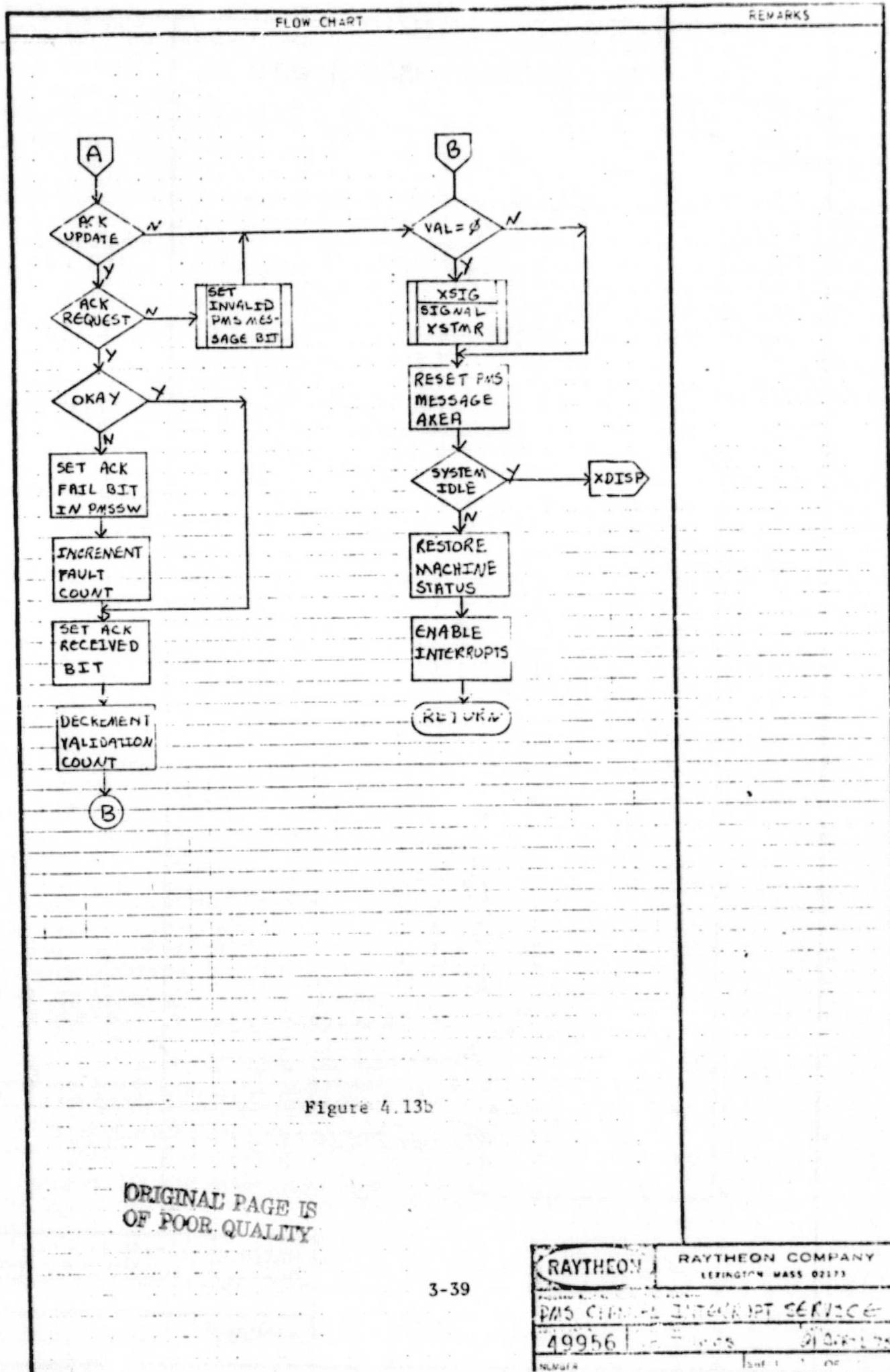
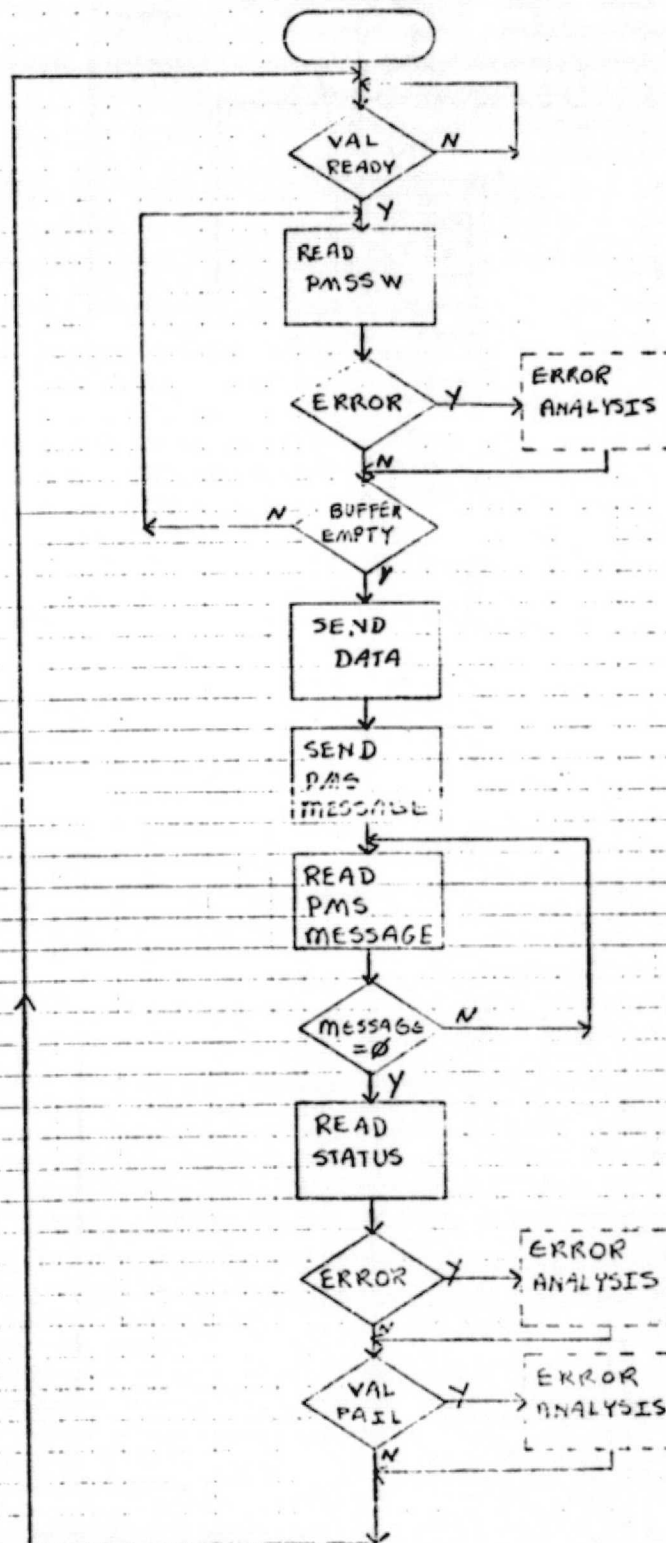


Figure 4.13b

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PMS CHANNEL HANDSHAKING



VALIDATION
DATA READY?

SYSTEM ERROR

CHECK APPROPRIATE
VALIDATION
"BUFFERS"

SEND VALIDATION
DATA

WAIT FOR CE
TO PROCESS
MESSAGE

INVALID PMS
MESSAGE

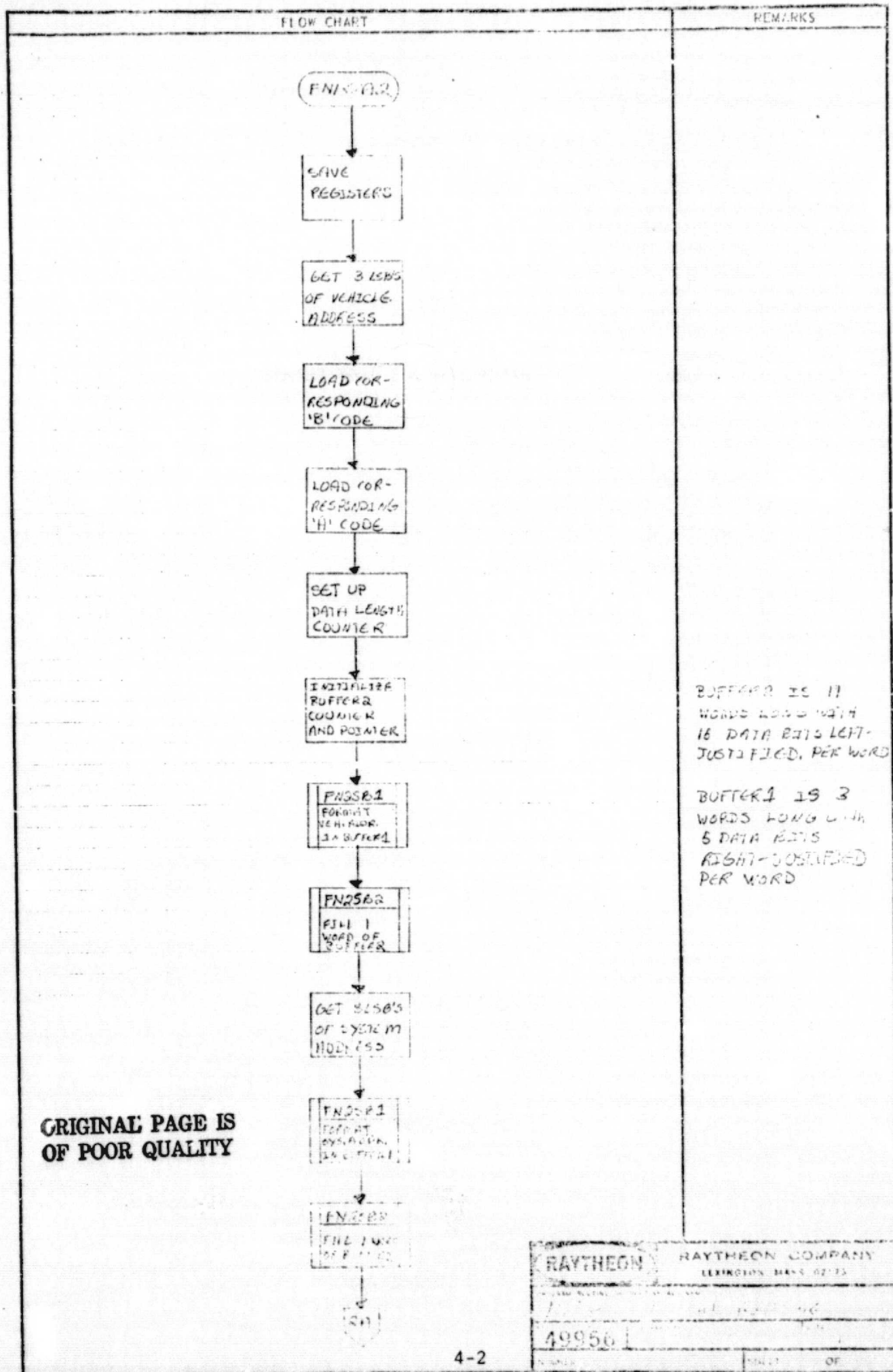
VALIDATION
FAILURE

Figure 4.14

RAYTHEON		RAYTHEON COMPANY LEXINGTON MASS 02173	
49956		DATE	
V.M. 15		SHEET OF	

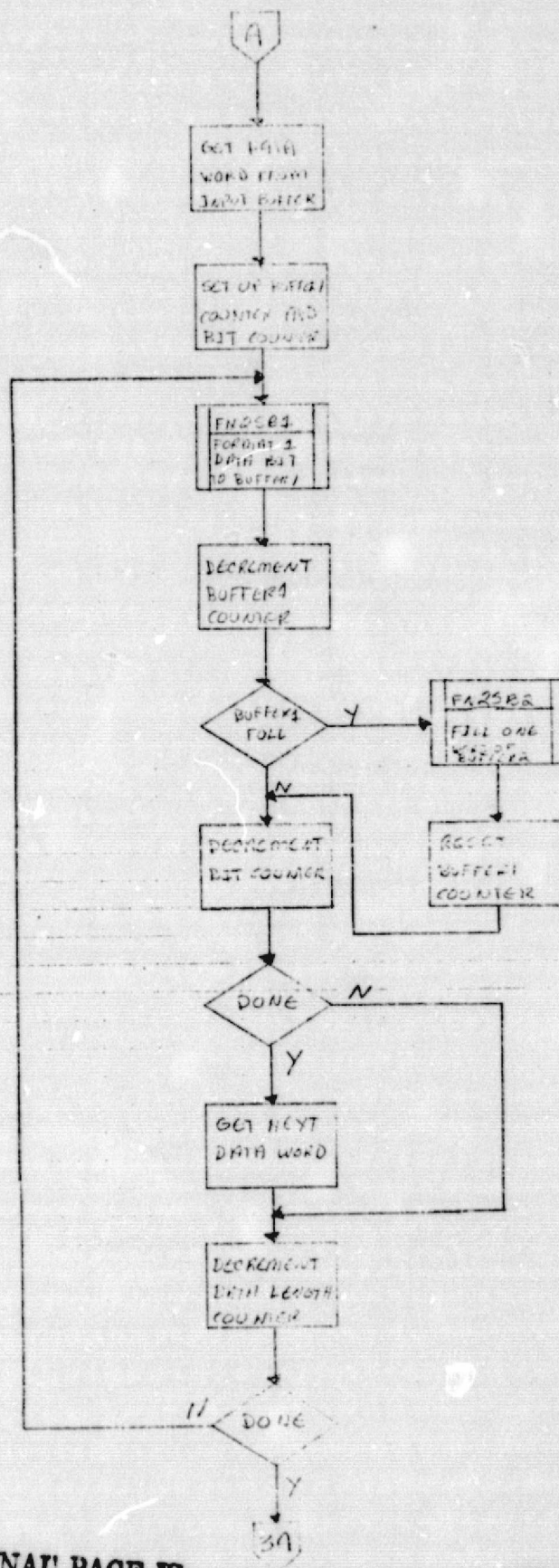
APPENDIX A

MISCELLANEOUS FLOW CHARTS



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RAYTHEON		RAYTHEON COMPANY	
		LEXINGTON, MASS. 02173	
49956			
REVISED		DATE	

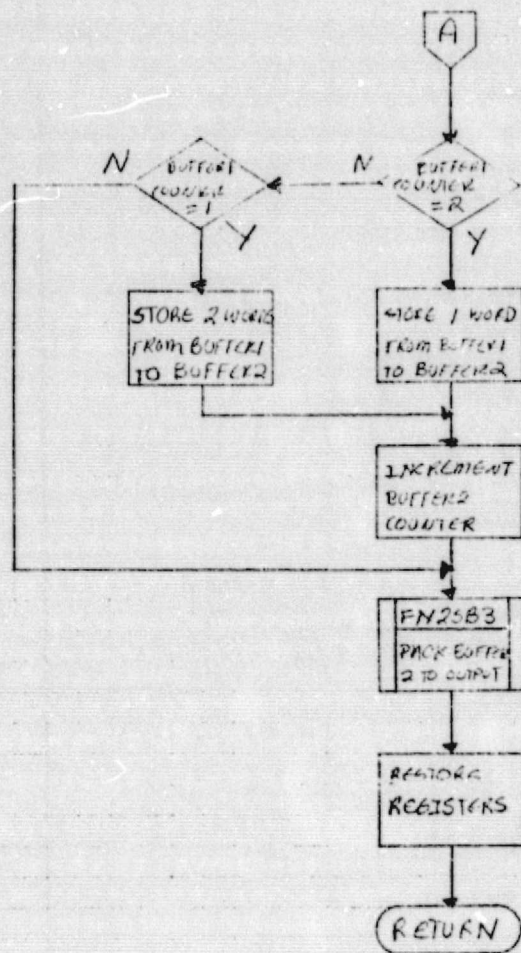


BUFFER COUNTER = 3
BIT COUNTER = 16

BIT COUNTER
DOES NOT HAVE
TO BE RESET;
NO MORE THAN
2 DATA WORDS

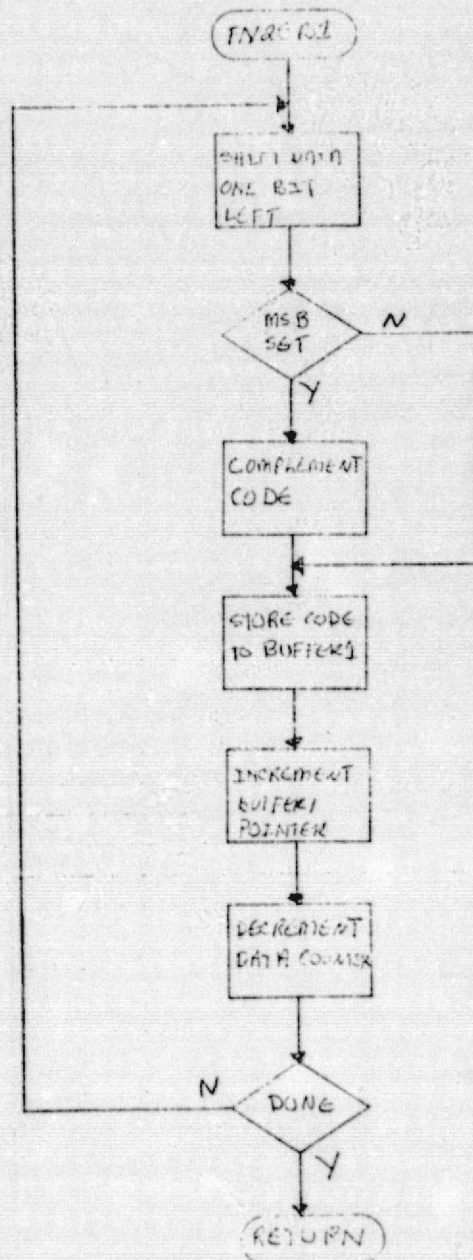
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RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS. 02173	
49956			
4-3			



RAYTHEON		RAYTHEON COMPANY	
		LEXINGTON MASS 02173	
PROGRAM ELEMENT IDENTIFICATION			
49956			
REVISION 1			

FILL BUFFER 1

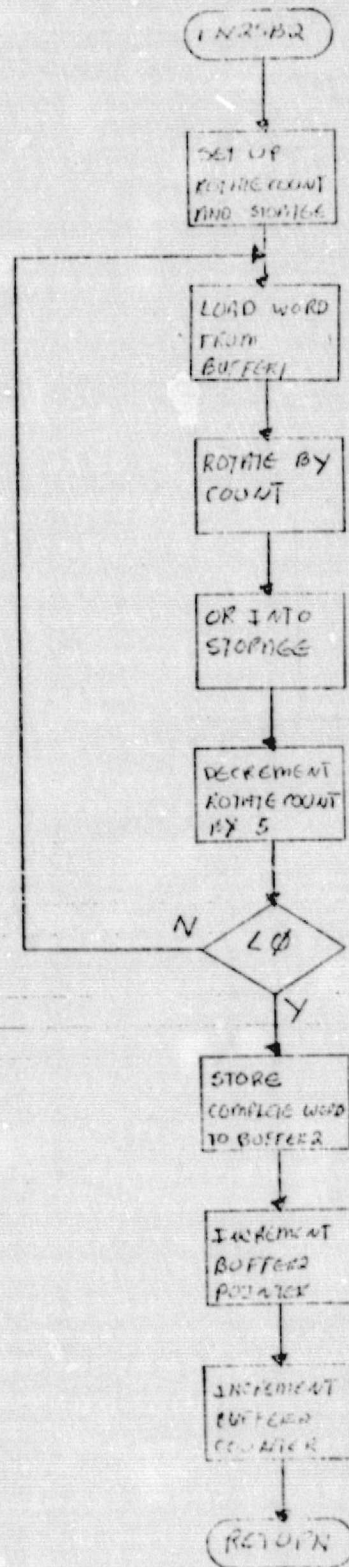


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RAYTHEON		RAYTHEON COMPANY LEXINGTON MASS 02173	
49956		DATE: 11-1-73	
BY: [Signature]		CHECKED: [Signature]	

FLOW CHART

REMARKS



FILL BUFFER 2

ROUTE COUNT = 11
STORAGE = 0

DONE 3 WORDS

RAYTHEON

RAYTHEON COMPANY
LEXINGTON, MASS 02173

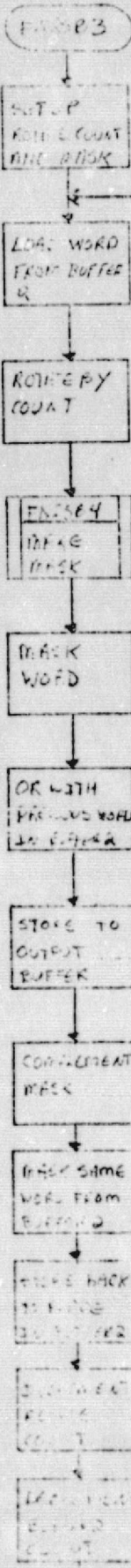
49956

FLOW CHART

REMARKS

DEFS OUTPUT
BUFFER 16 BYTES/WORD

ROUTINE COUNT = 1
MASK = 0

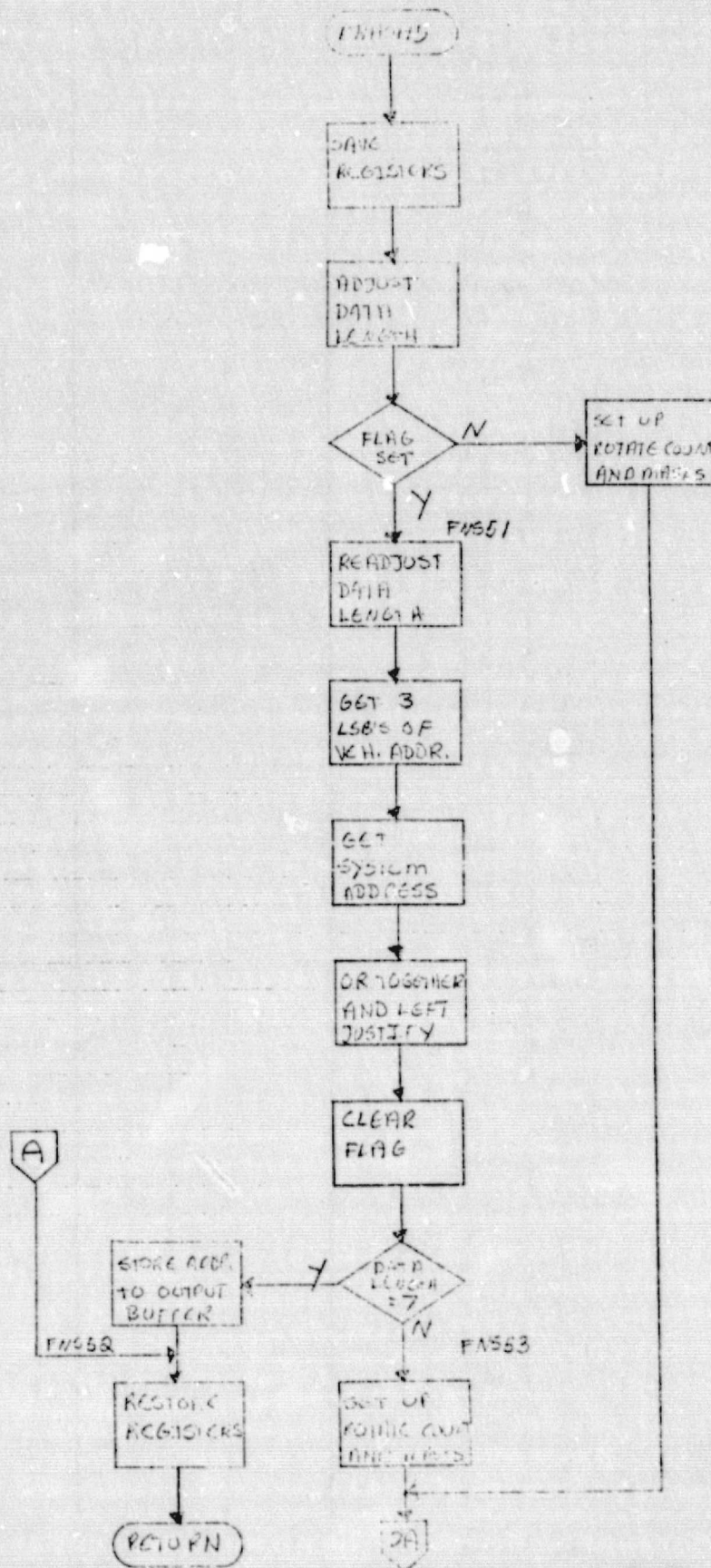


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RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS 02173
49956	
JUL 10 1964	

FLOW CHART

REMARKS



SUBPACT 7

FLAG SET =>
ADD ADDRESSES

ROTATE COUNT = 0
MASK 1 = 177777
MASK 2 = 0

ADD 7

ROTATE COUNT = -7
MASK 1 = 1770000
MASK 2 = 000777

RAYTHEON

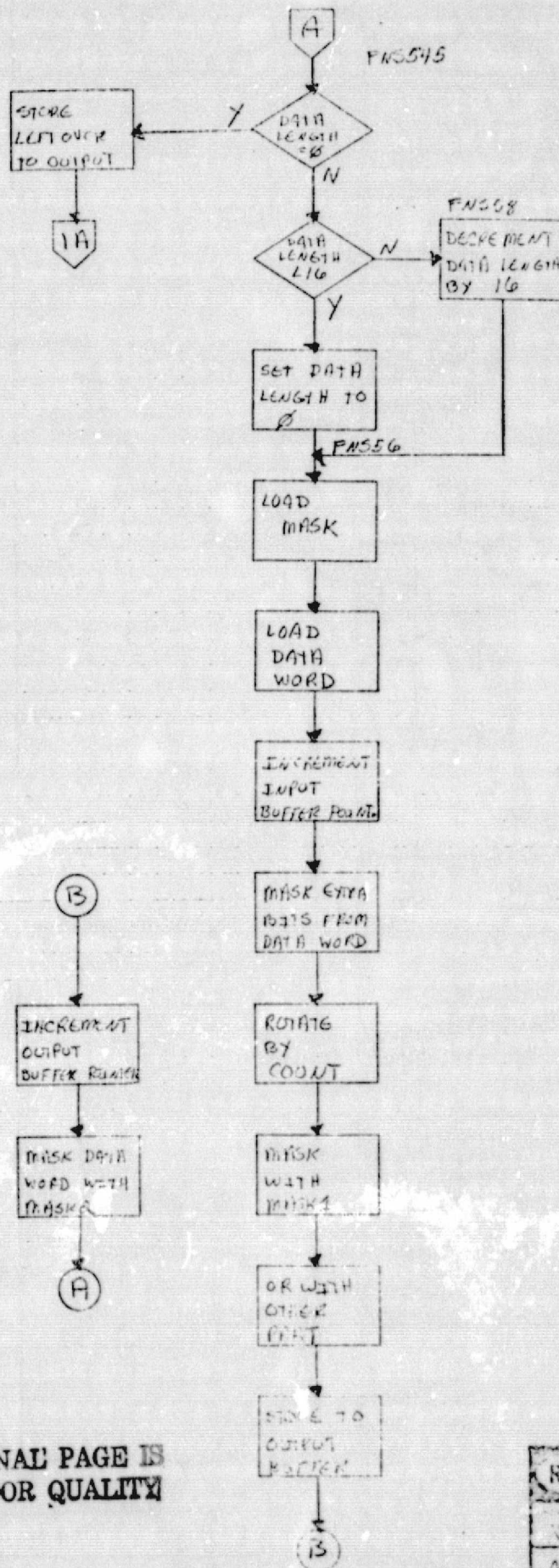
RAYTHEON COMPANY
LEXINGTON MASS 02173

7-11-51

48956

FLOW CHART

REMARKS



FIRST TIME, OTHER PART IS NECESSARY OR 0.

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RAYTHEON		RAYTHEON COMPANY LExINGTON, MASS 02173	
49956			
49956			

FLOW CHART

REMARKS

FDODH

SAVE
REGISTERS

RESERVE
STACK
LOCATIONS

GET 3456
OF SYSTEM
ADDRESS

LOAD 1st
DATA
WORD

INCREMENT
INPUT BUFFER
POINTER

ROTATE AND
MASK DATA
WORD

OR WITH
SYSTEM
ADDRESS

FFDRTY
PARITY ON
16 BITS

STORE WORD
TO OUTPUT
BUFFER

INCREMENT
OUTPUT BUFFER
LOCATION

MARK 1st
DATA WORD
AS SET

20

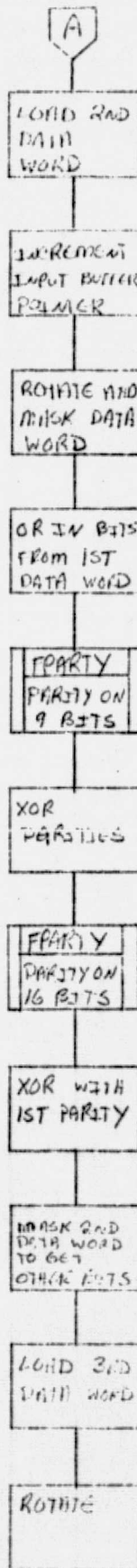
RAYTHEON

RAYTHEON COMPANY
LEXINGTON MASS 02173

40956

FLOW CHART

REMARKS



BITS 1-16 WITH
BITS 17-32

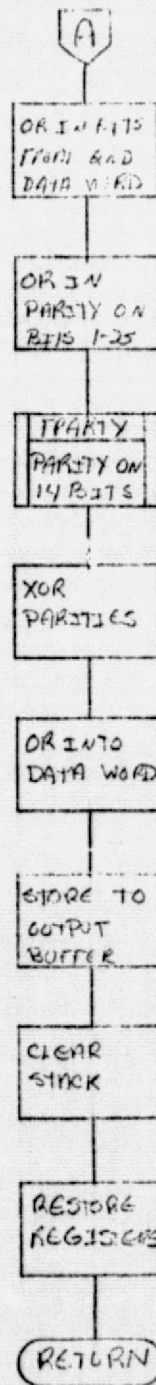
BITS 1-16
BITS 17-32

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RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02172	
DND 11 100-100-100		100-100-100	
49956		100-100-100	
4-11		100-100-100	

FLOW CHART

REMARKS

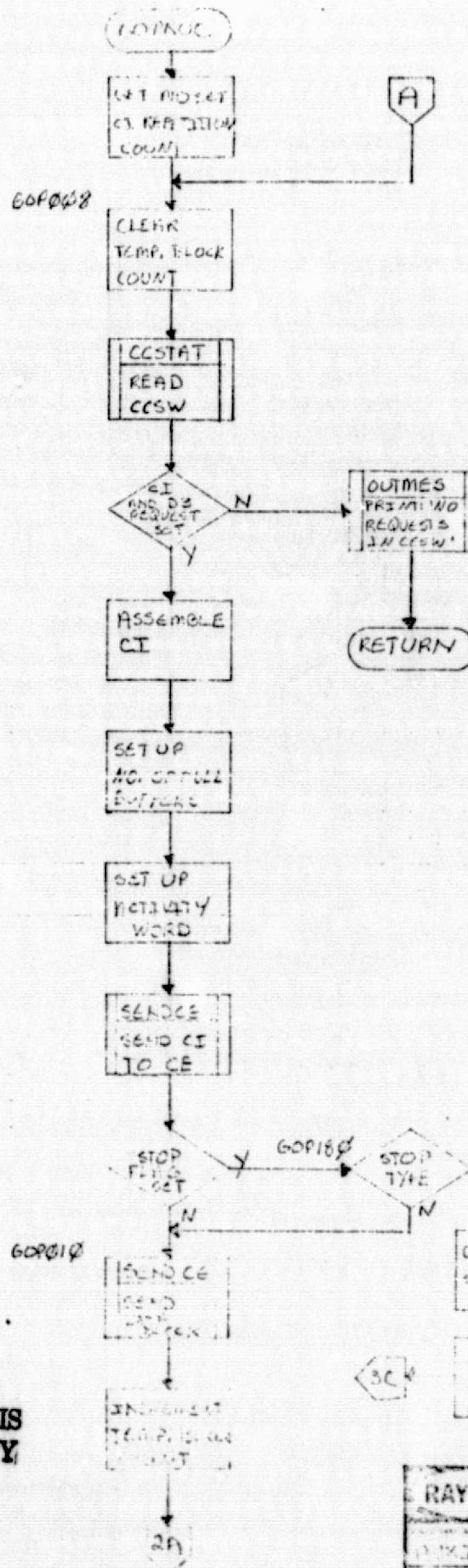


BITS 1-32 WITH
BITS 33-46

RAYTHEON

RAYTHEON COMPANY
LEXINGTON MASS 02172

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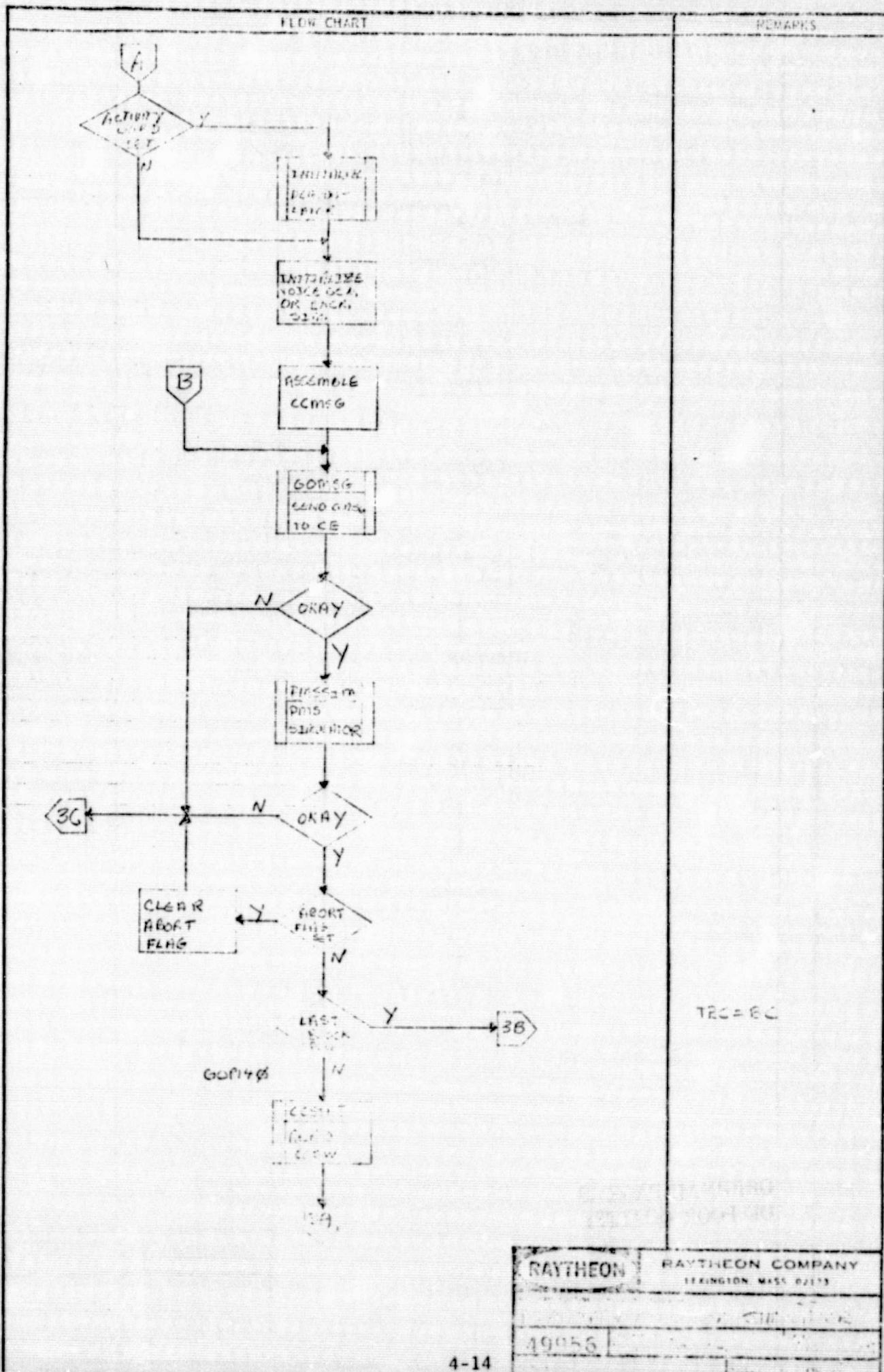


IO OPTION PR MUST HAVE 16 BUFFERS; VALIDATIONS MUST HAVE 1 BUFFER.

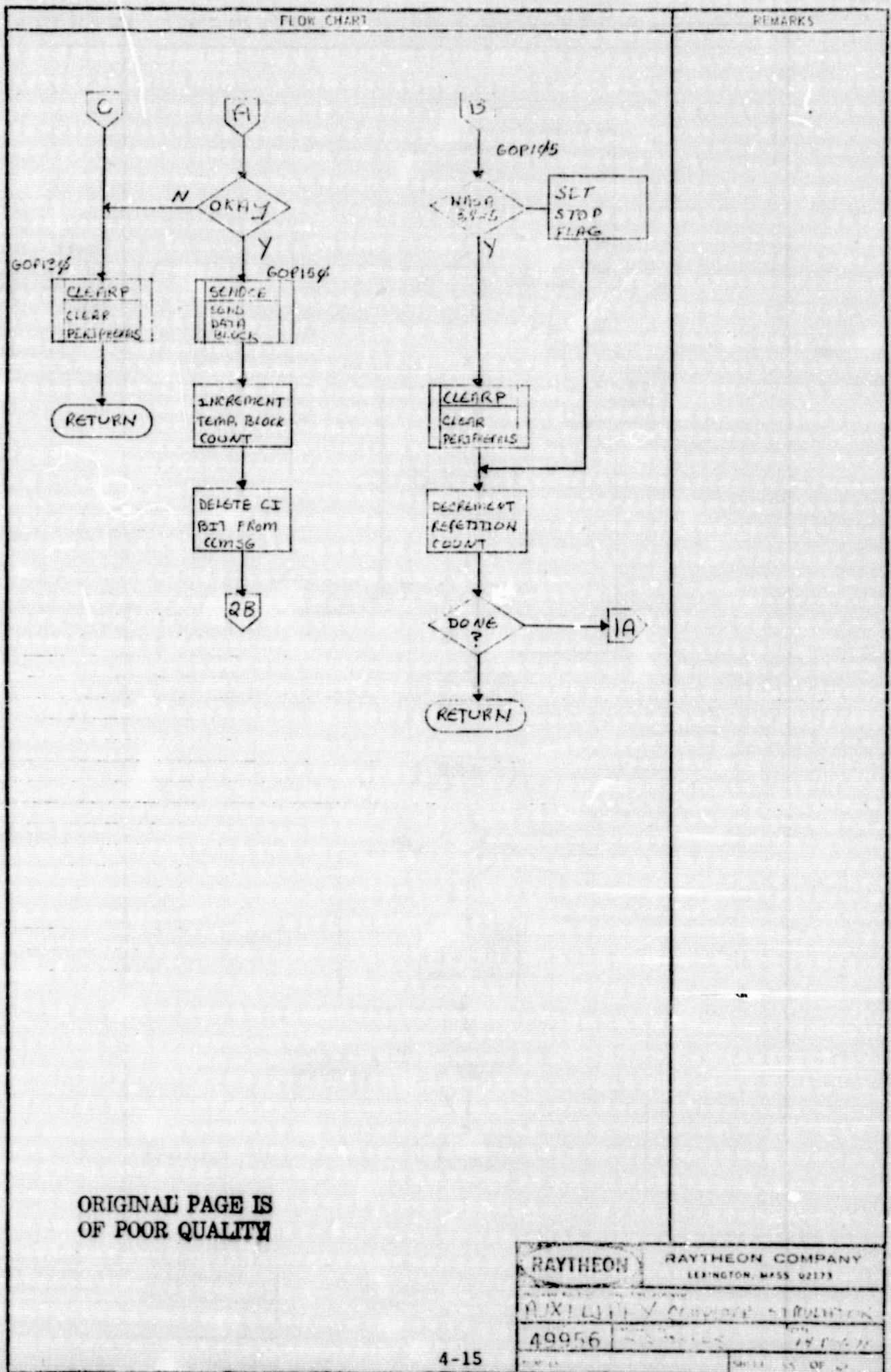
DSVAL= VERIFICATION REQUEST U VALIDATION U PR OPTION IN TO REQUEST.

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RAYTHEON		RAYTHEON COMPANY	
		LEXINGTON MASS 02173	
49956		1-10-75	

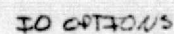
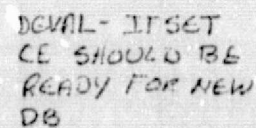


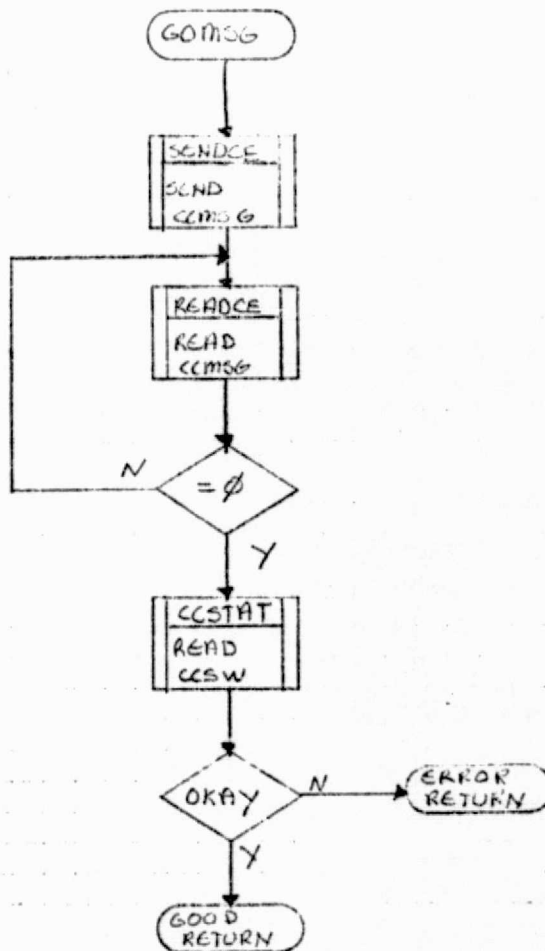
RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS 02173
49056	



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RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS 02173
AUXILIARY COMPANY INFORMATION	
49956	18757
SHEET 55 OF 57	

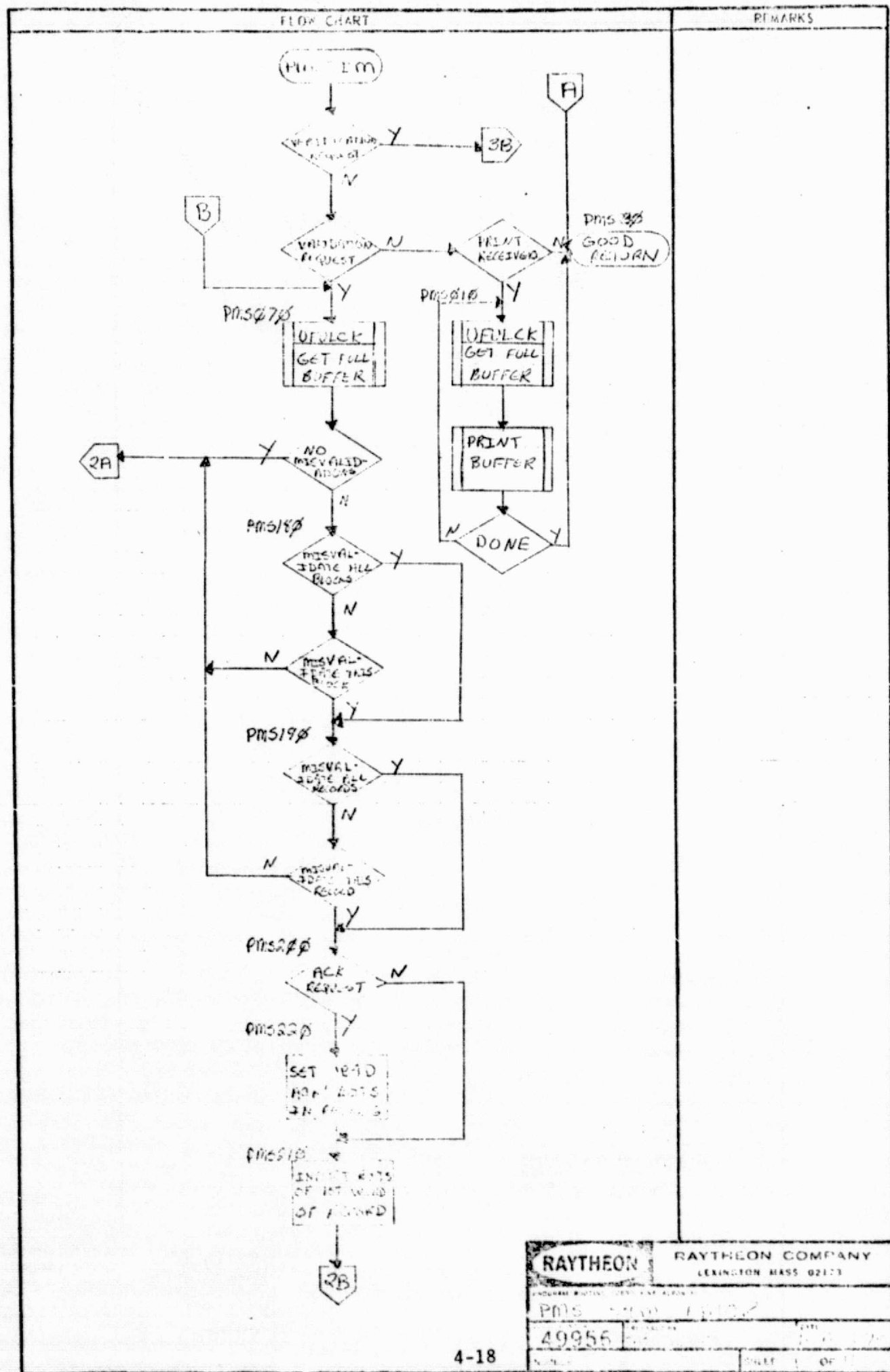




MESSAGE HAS
BEEN RECEIVED
BY CE

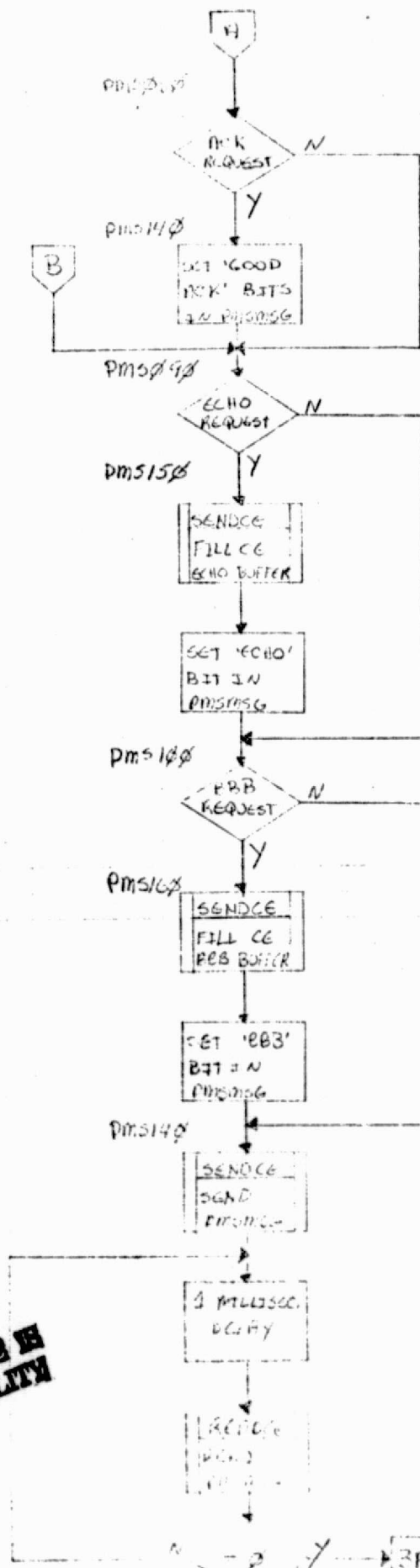
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RAYTHEON		RAYTHEON COMPANY LEXINGTON MASS 02173	
49956		RAYTHEON COMPANY	
4-17		4-17	



FLOW CHART

REMARKS

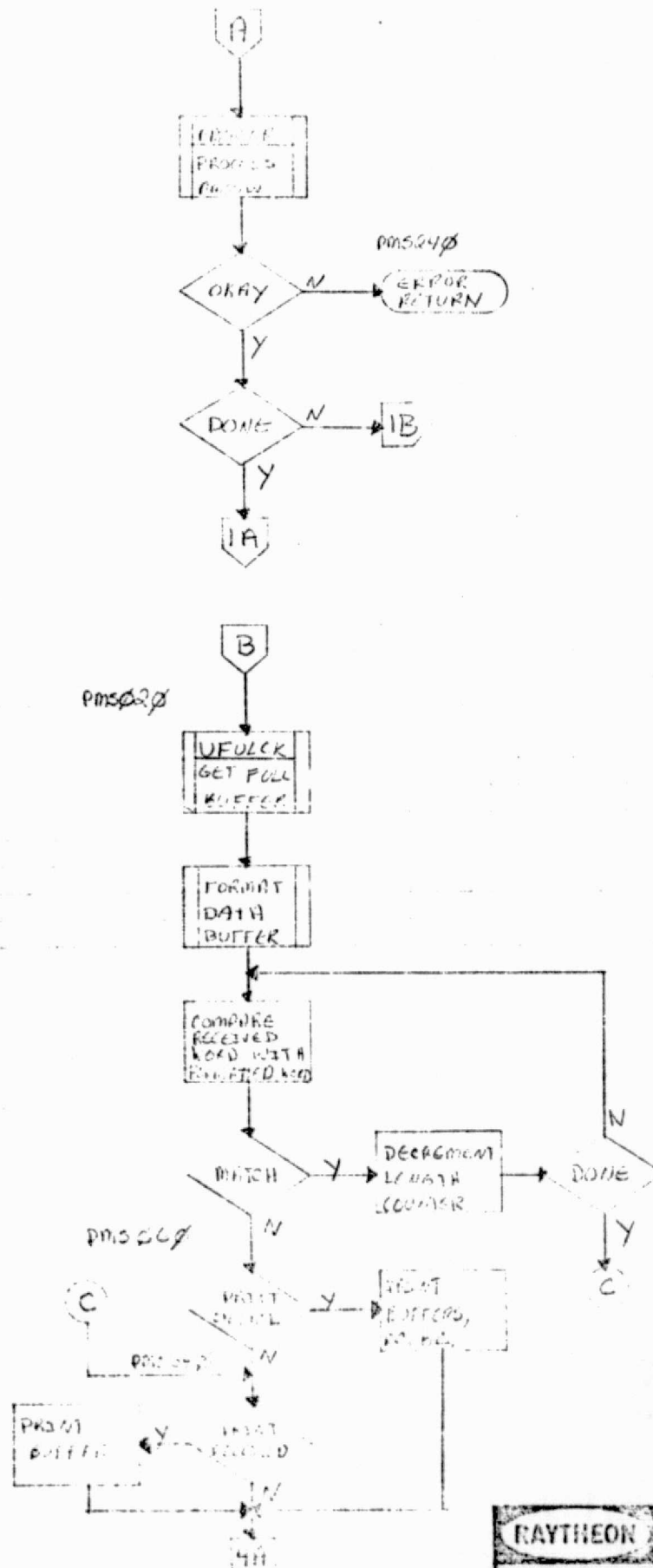


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RAYTHEON		RAYTHEON COMPANY	
LEXINGTON, MASS 02173			
49956			
SHEET		OF	

FLOW CHART

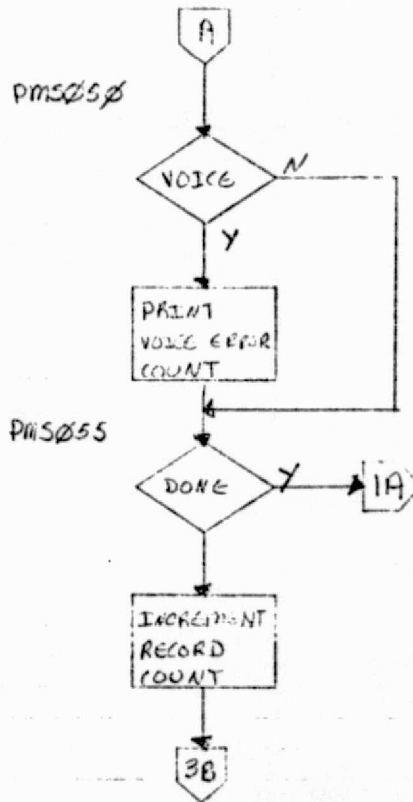
REMARKS



RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02173	
PART NO. 49956			
REV. 1		DATE 7-5	
DRAWN BY		CHECKED BY	

FLOW CHART

REMARKS



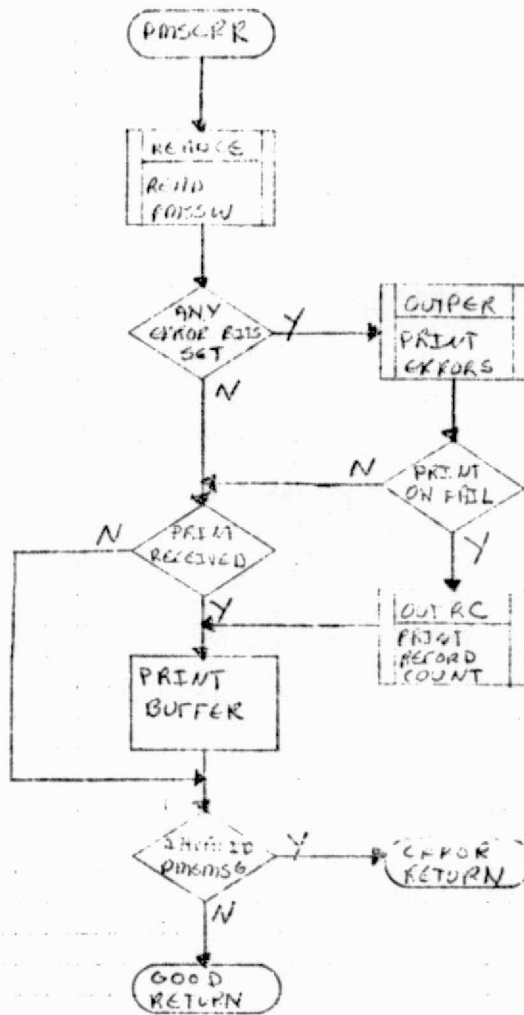
INCLUDED IN
AND REPLACED
BY MSG-CTL
ROUTINE

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RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02172	
49956			
DATE		PAGE 14 OF 44	

FLOW CHART

REMARKS



RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS 02173	
49956		111	
4-22		111 / 111	

APPENDIX BTABLE 1

<u>FORMAT/MODULATION</u>	<u>TYPE CODE</u>	
NASA 1		
WITHOUT VOICE	00000	(0)
WITH VOICE	00001	(1)
STOP	00010	(2)
NASA 2		
SP = # bits/input record	00100	(4)
STOP	00010	(2)
NASA 3		
1 EXEC WORD	01000	(8)
2 EXEC WORDS	01001	(9)
3 EXEC WORDS	01010	(10)
NASA 4	01011	(11)
NASA 5		
STANDARD (without address)	01100	(12)
MEMORY LOAD (with address)	01101	(13)
NASA 6		
WITHOUT VOICE	01111	(15)
STOP	00010	(2)
DOD1	10001	(17)
DOD2	10010	(18)
DOD3	10011	(19)
DOD4	10100	(20)
DOD5	10101	(21)
DOD6	10110	(22)

TABLE 1 (Continued)

<u>FORMAT/MODULATION</u>		<u>TYPE CODE</u>	
DOD7		10111	(23)
DOD8		11000	(24)
DOD9		11001	(25)
DOD10		11010	(26)
DOD11		11011	(27)
DOD12		11100	(28)
DOD13		11101	(29)
STOP		00010	(2)
UNUSED TYPE CODES:			
	00011	(3)	
	00101	(5)	
	00110	(6)	
	00111	(7)	
	01110	(14)	
	10000	(16)	
	11110	(30)	
	11111	(31)	

TABLE 2

NASA 3 EXECUTE FREQUENCY TABLE

MTBN3E	DC	MTBN3E		
	DC	2000	EXECUTE TONE	1
	DC	2270		2
	DC	2650		3
	DC	3000		4
	DC	3305		5
	DC	3621		6
	DC	3850		7

TABLE 3

NASA 3 ADDRESS FREQUENCY TABLE

MTBN3A	DC	MTBN3A		
	DC	1025	ADDRESS TONE	1
	DC	1097		2
	DC	1174		3
	DC	1262		4
	DC	1352		5
	DC	1447		6
	DC	1549		7
	DC	1750		8
	DC	1860		9
	DC	4245		10
	DC	4550		11
	DC	5155		12
	DC	5451		13
	DC	5790		14
	DC	6177		15

TABLE 4

NASA 4 VEHICLE FREQUENCY TABLE

MTN4F	DC	7100	VEHICLE	0
	DC	7200		1
	DC	7400		2
	DC	7600		3
	DC	7800		4
	DC	8000		5
	DC	8200		6
	DC	8400		7
	DC	8600		8
	DC	8800		9
	DC	9000		10
	DC	9200		11
	DC	9400		12
	DC	9600		13
	DC	9800		14
	DC	10000		15

TABLE 5
NASA 5 VEHICLE DEPENDENT DATA

MTBN5	DC	0 Freq.	1 Freq,	Modulation Freq,	Bit Delay*
	DC	7000,	14000,	32, 0	Vehicle 0
	DC	9000,	11000,	32, 4	1
	DC	11000,	15000,	128, 2	2
	DC	18000,	13000,	512, 2	3
	DC	15000,	20000,	100, 4	4
	DC	15000,	21000,	300, 2	5
	DC	21000,	14000,	300, 2	6
	DC	20000,	9000,	800, 0	7
	DC	18000,	11000,	512, 4	8
	DC	12000,	20000,	512, 2	9
	DC	14000,	19000,	16, 0	10
	DC	12000,	17000,	64, 4	11
	DC	10000,	19000,	256, 2	12
	DC	8000,	21000,	1024, 4	13
	DC	9500,	14500,	16, 4	14
	DC	15500,	7777,	64, 2	15

* Bit Delay Codes: 0 = 1/2 Bit Delay
 2 = 1/4 Bit Delay
 4 = 0 Bit Delay

TABLE 6

NASA 6 LOOK UP TABLE FOR SUBCARRIER AND MODULATION FREQS

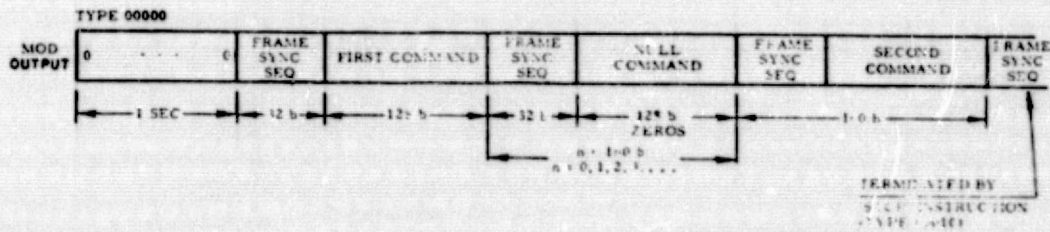
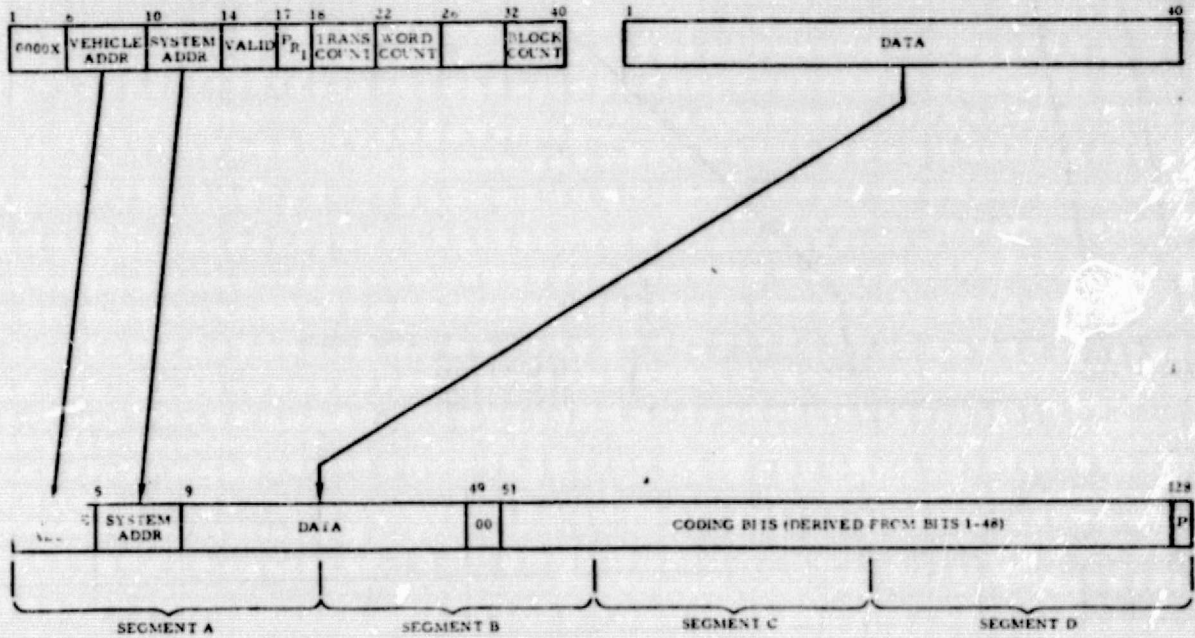
MTBN6	DC	2,1	SUB, MOD FOR VEHICLE	
	DC	4,2		1
	DC	8,4		2
	DC	16,8		3
	DC	32,16		4
	DC	64,32		5
	DC	128,64		6
	DC	256,128		7
	DC	512,256		8
	DC	1024,512		9
	DC	2048,1024		10
	DC	4096,2048		11
	DC	2,1		12
	DC	4,1		13
	DC	8,2		14
	DC	16,4		15

APPENDIX C

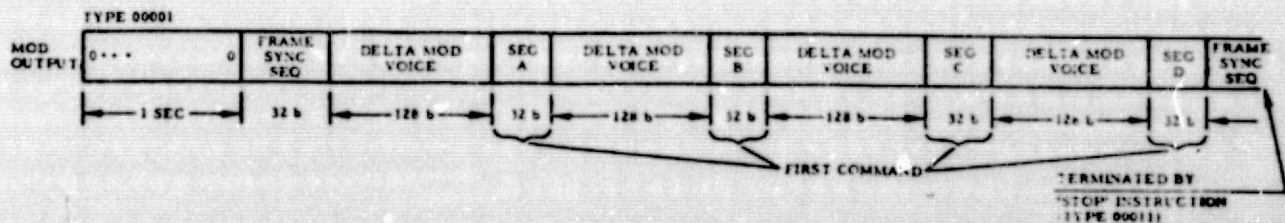
Formatting Summary

The formatting and coding functions implemented by the Coding and Format Generation Unit are summarized as follows:

NASA 1 (ENCODED BI-Ø-L)



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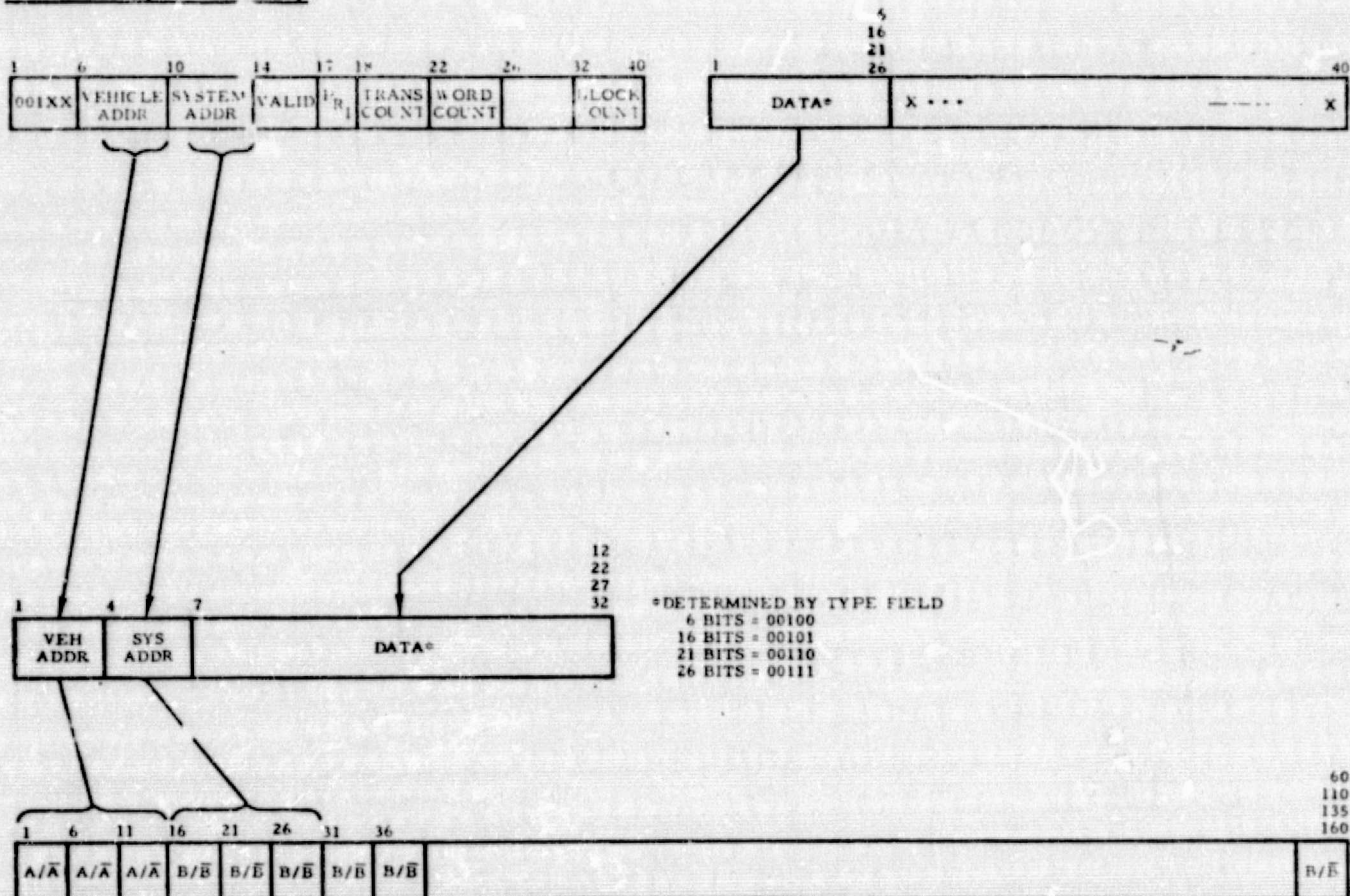


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NASA 2 (APOLLO)



A, B ARE 5-BIT BINARY PATTERNS DETERMINED BY VEHICLE ADDRESS

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NASA 3 (TONE STANDARD)

1	6	10	14	17	19	22	25	32	40
010XX	VEHICLE ADDR	SYSTEM ADDR	VALUE	TRANS COUNT	WORD COUNT			BLOCK COUNT	

1	4	7	10						00
EXEC WORD	EXEC WORD	EXEC WORD	X	...					X

QUANTITY OF EXEC WORDS
DETERMINED BY TYPE FIELD
01000 - NOT USED
01001 - 1 WORD
01010 - 2 WORDS
01011 - 3 WORDS

1	5	8	11	13
ADDR	EXEC WORD 1	EXEC WORD 2	EXEC WORD 3	

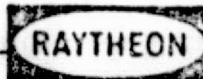
(0000 NOT USED)

(0000 NOT USED)

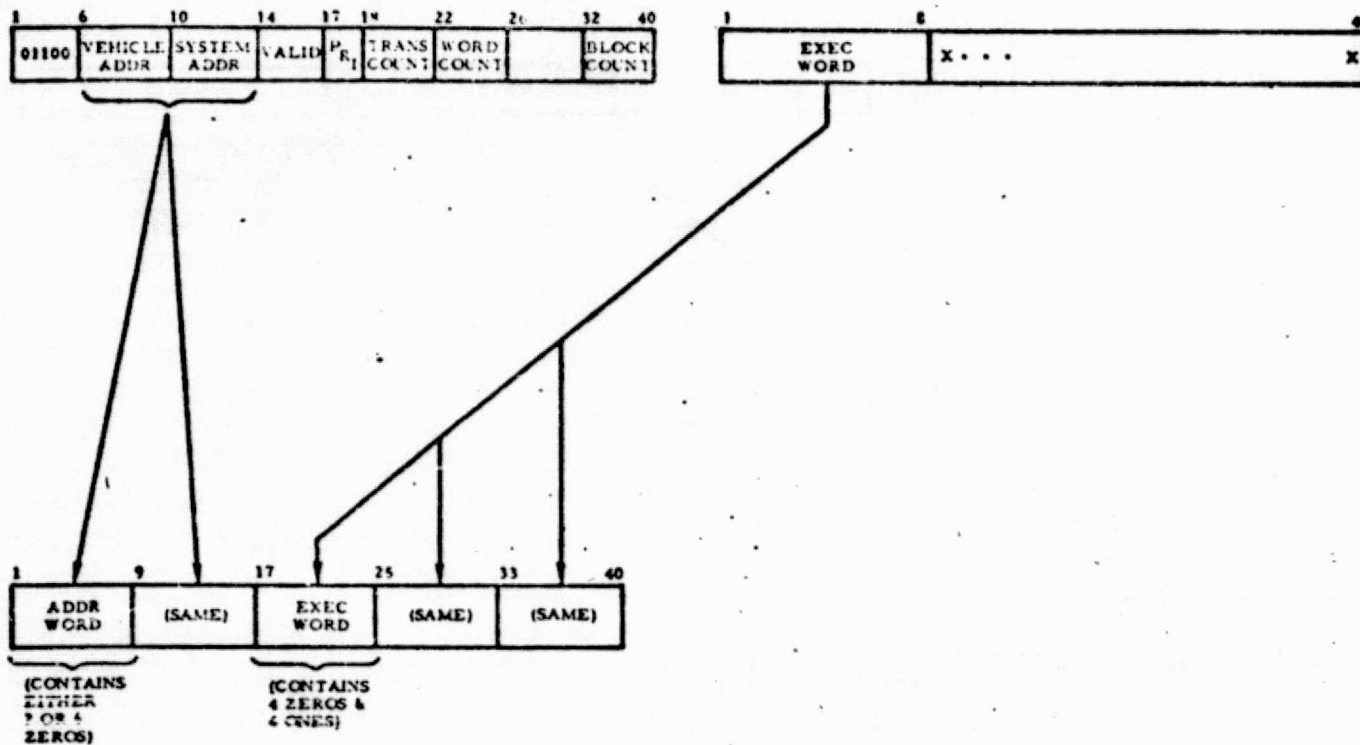
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NASA 4 (TONE DIGITAL STANDARD)

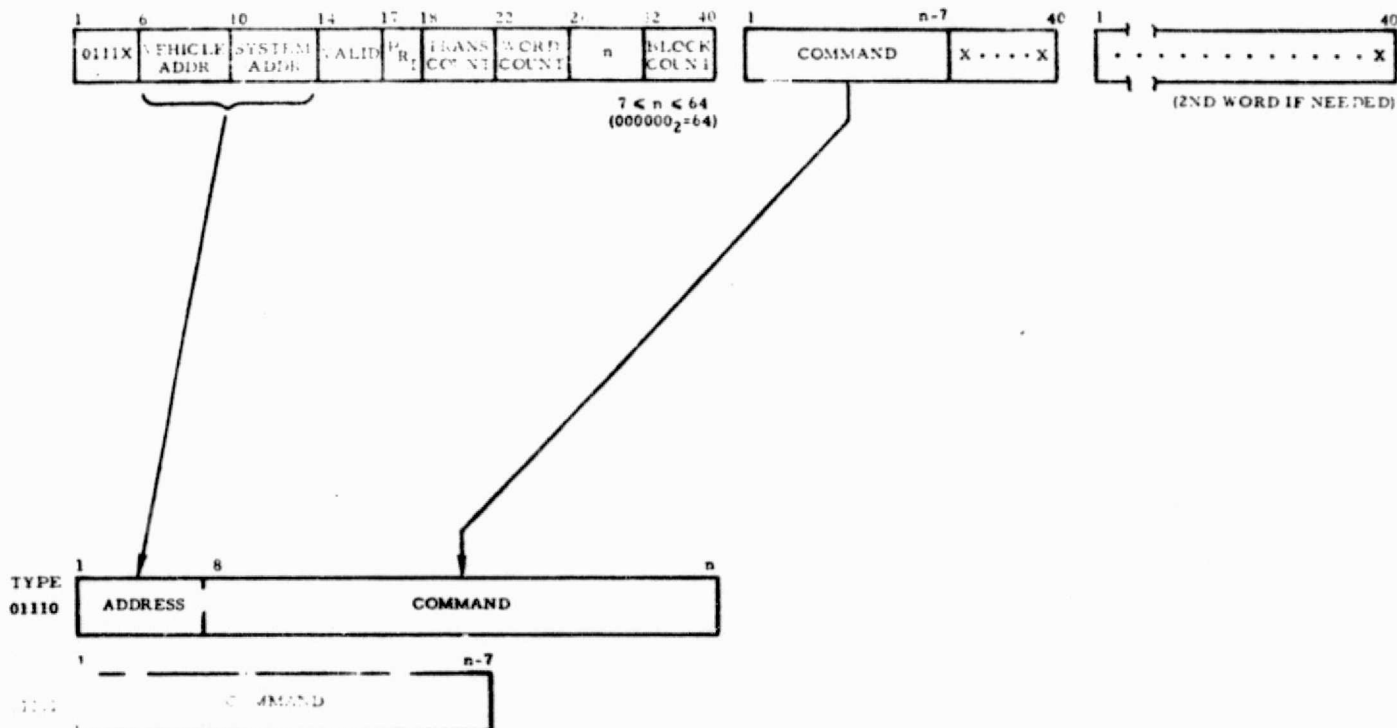


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NASA 5 (PCM/FSK STANDARD)



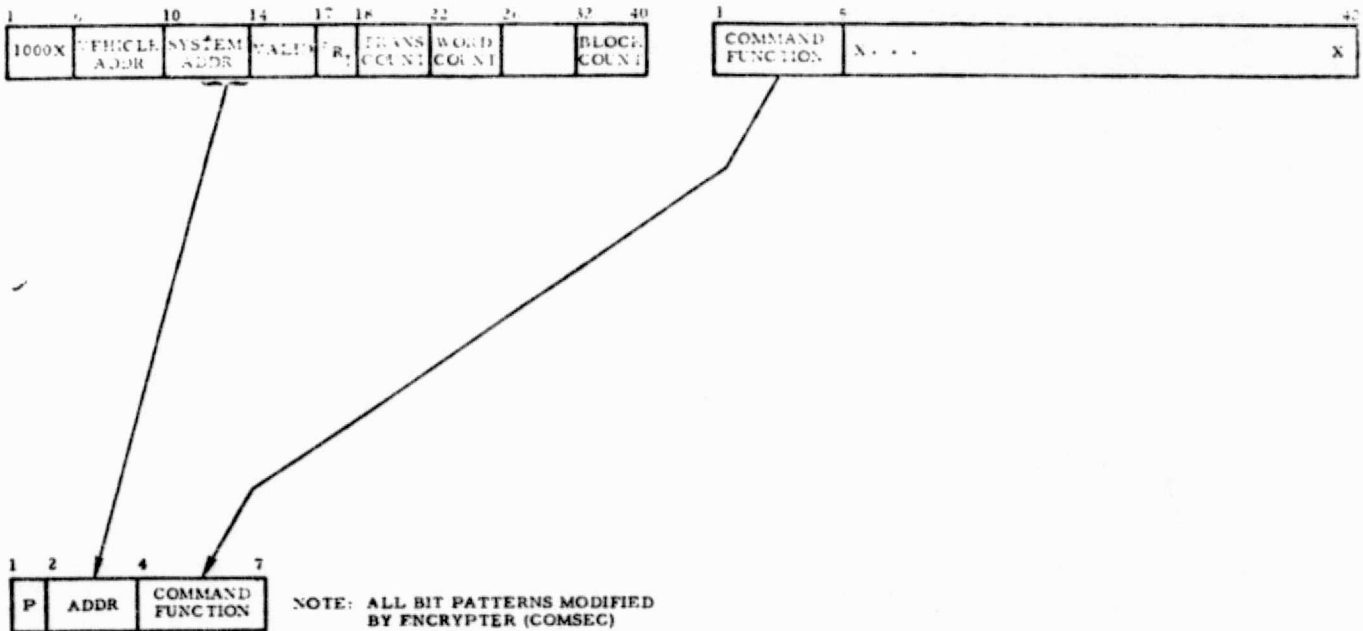
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DOD 1 (7 BIT COMMAND)

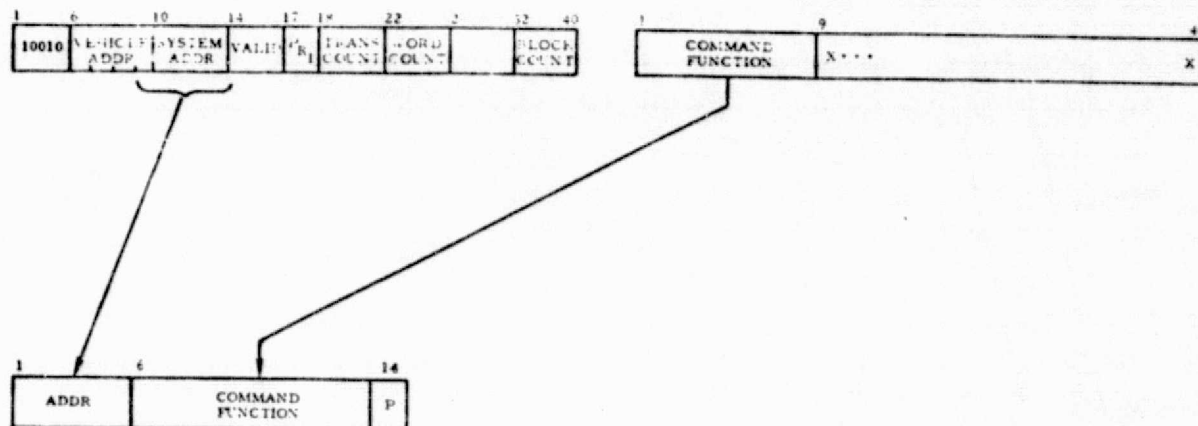


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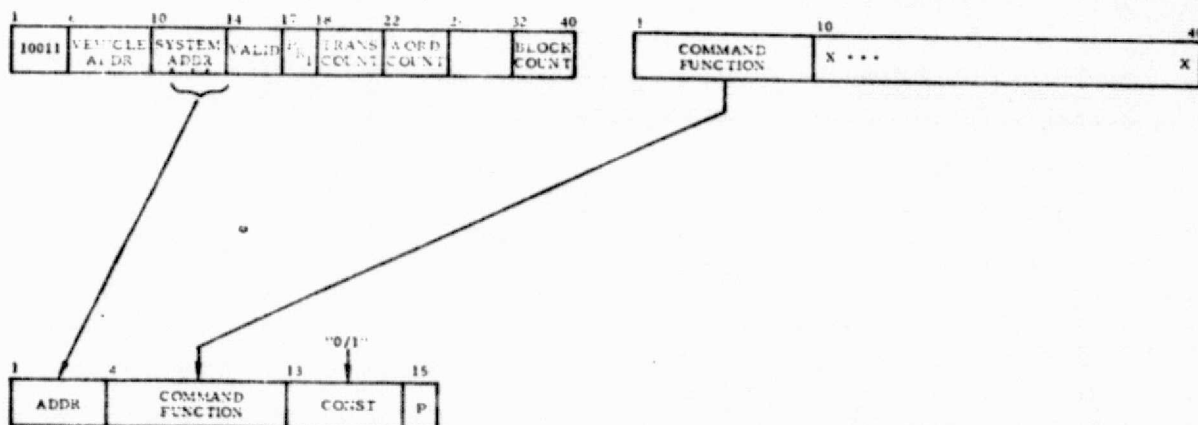
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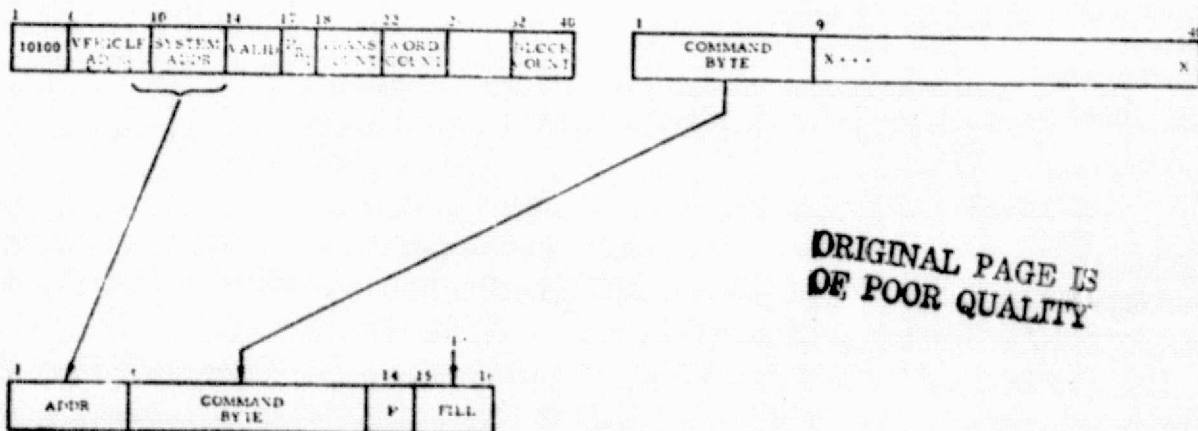
DOD 2 (14 BIT COMMAND)



DOD 3 (15 BIT COMMAND)



DOD 4 (16 BIT COMMAND)



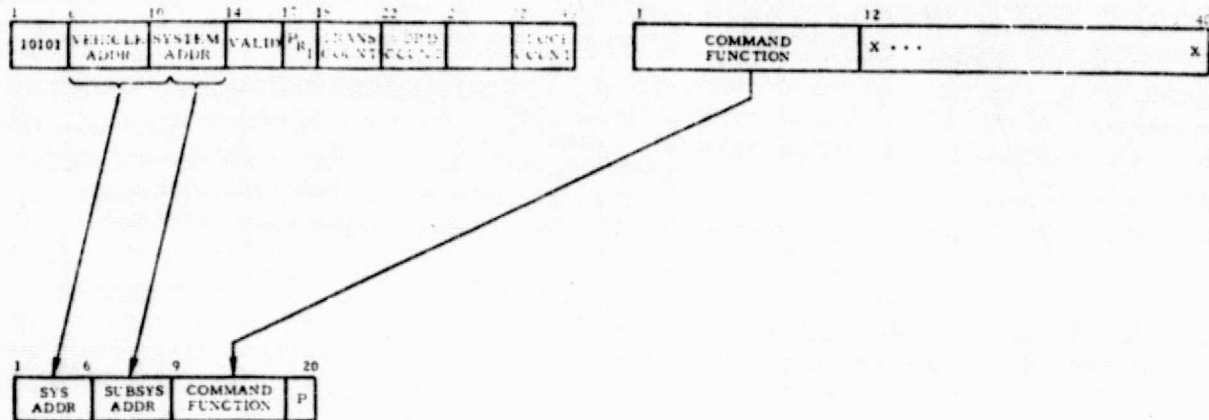
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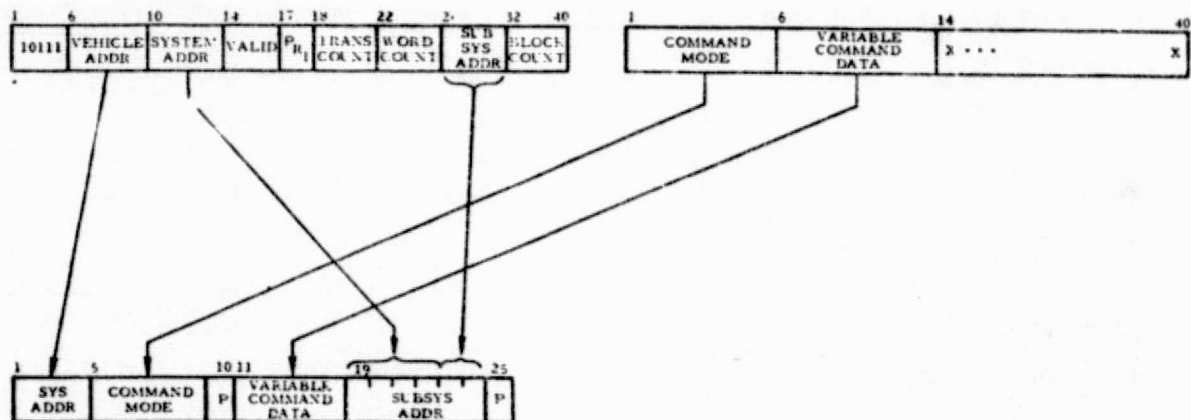
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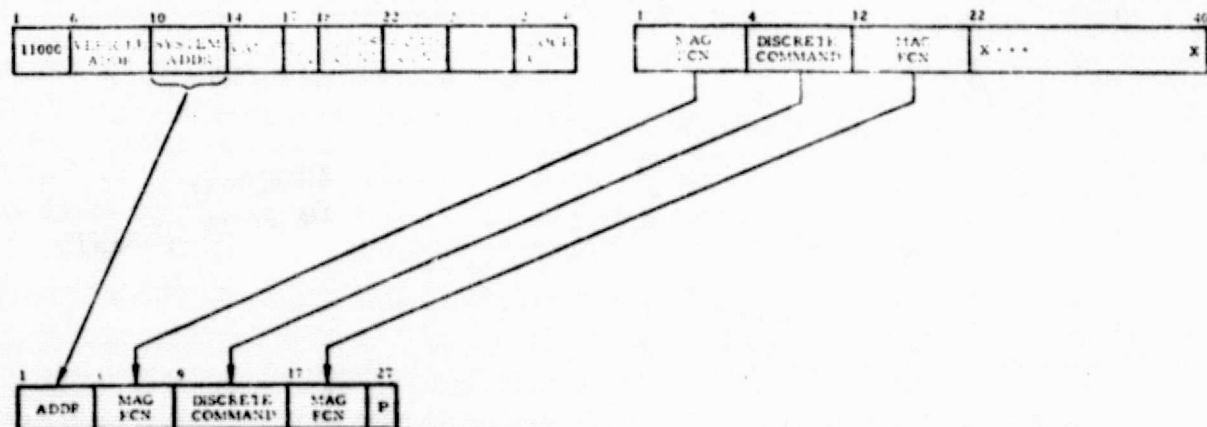
DOD 5 (20 BIT COMMAND)



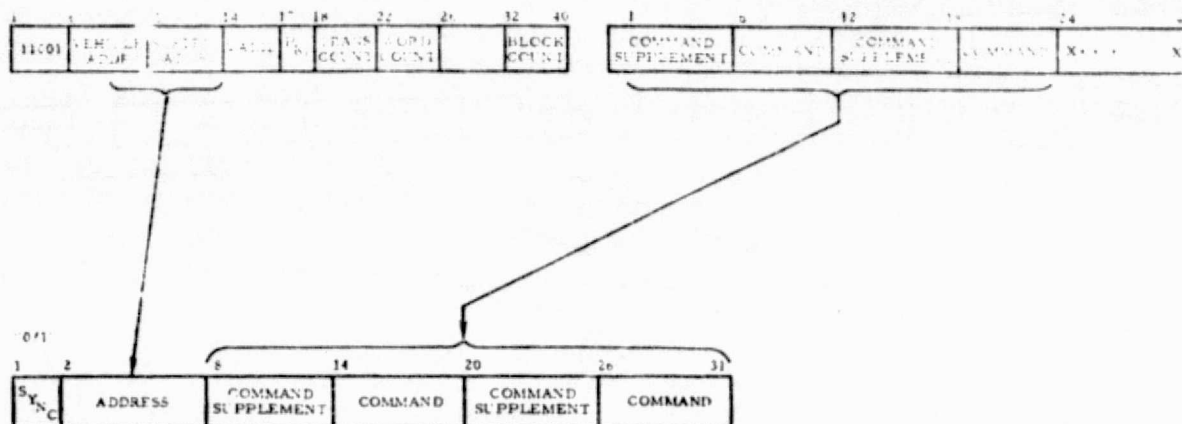
DOD 6 (25 BIT COMMAND)



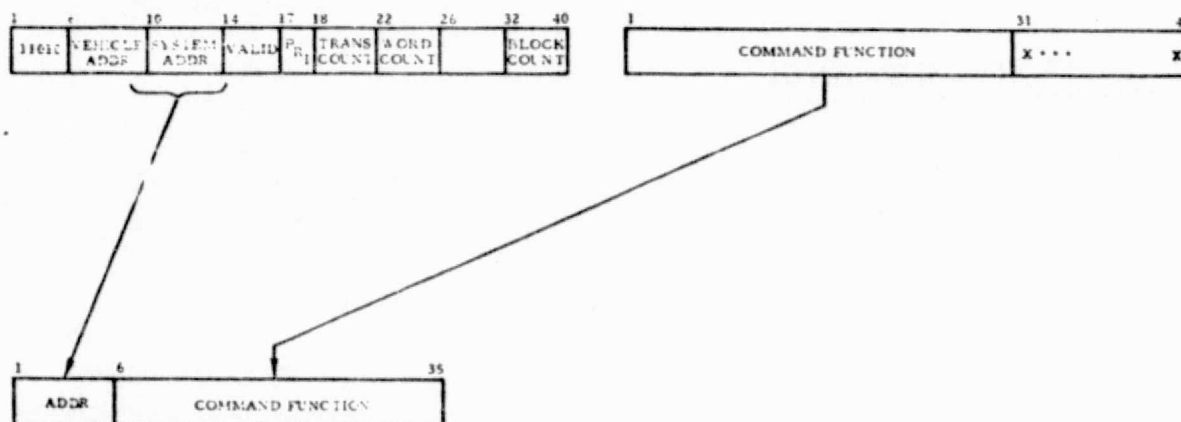
DOD 7 (27 BIT COMMAND)



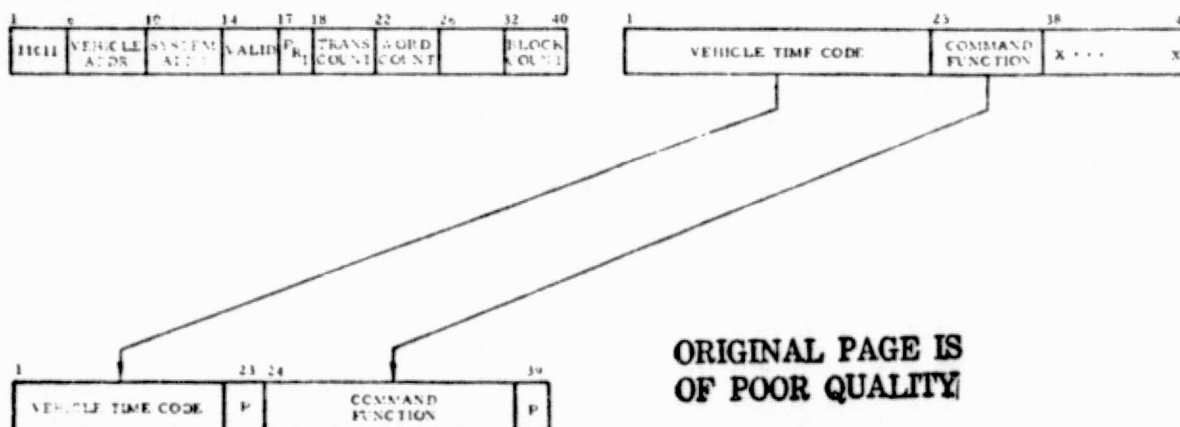
DOD 8 (31 BIT COMMAND)



DOD 9 (35 BIT COMMAND)



DOD 10 (39 BIT COMMAND)



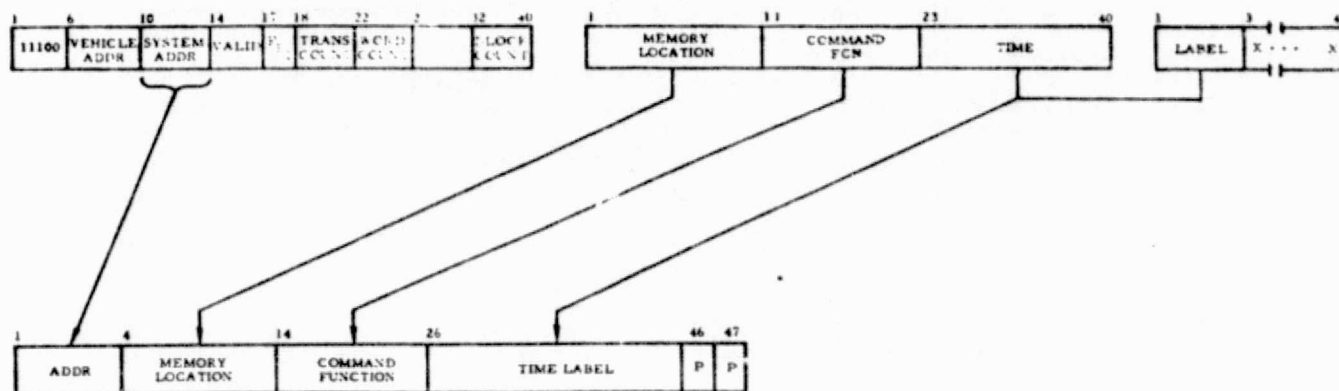
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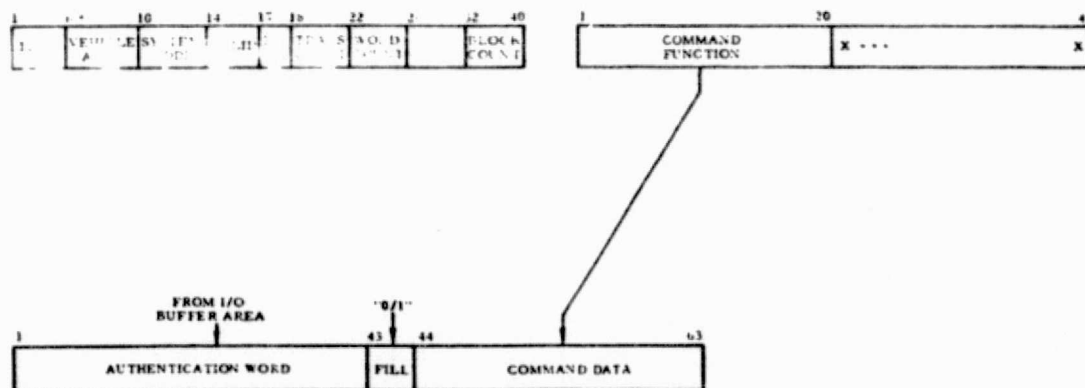
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DOD 11 (47 BIT COMMAND)



DOD 12 (63 BIT COMMAND)



DOD 13 (64 BIT COMMAND)

